New Products & Technologies

CAD System for Application Specific Custom Products*

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1 Outline

A CAD system for designing submicron ASICs (application specific integrated circuits) has been developed. This is an easy-to-use integrated CAD system structured by combining commercially available top-level CAD tools with original tools of Kawasaki Steel Corp. In order to cope with the increasing gate size and speed of ASICs, top-down design, in addition to conventional gate level design, has been made possible. The test method of CrossCheck Technology Inc. is employed to substantially reduce the development time of fault coverage test patterns.

2 EWS-base Integrated Design Environment

Taking advantage of high quality EWS-base CAD tools on the market, we structured an integrated design environment, using commercially available tools as the nucleus and adding our original ones. This approach has made it possible to make an integrated design from system to layout designs all on an EWS. **Figure 1** shows the ASCP design flow. **Figure 2** shows the CAD configuration.

For integration, the framework technology of Cadence has been used to customize the system so that Cadence tools, CADs available on the market, and our original tools can be started from the menu in the same manner of operation. In addition, use of a common data base makes it possible to check the results of analysis obtained with our tools against circuit diagrams input with Cadence tools. This improves operability and efficiency.

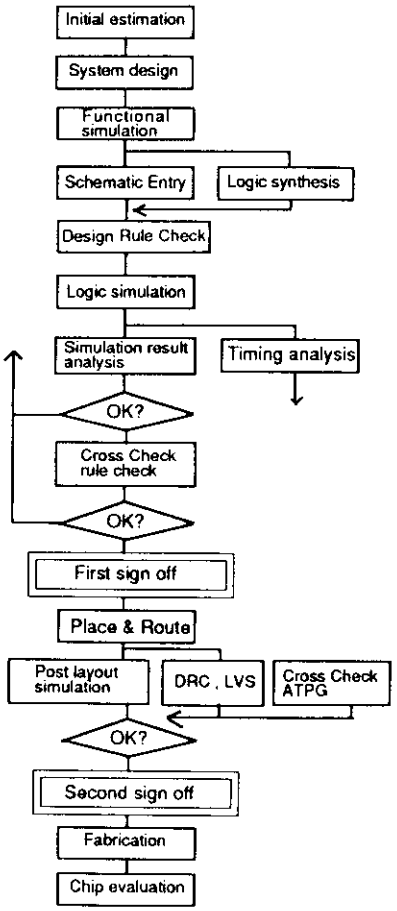

Fig. 1 ASCP design flow

3 Top-down Design Environment

An increase of design size results in an increase of design time as long as conventional gate level bottom-up design is pursued, making it increasingly difficult to complete a design within the desired turnaround time. In order to cope with this problem, top-down design by means of HDL (hardware description language) has recently attracting attention.

Basic components involved in top-down design are HDL, a logic synthesis tool, and an HDL simulators. The top-down design environment has been structured using Verilog-HDL as the HLD language, Synopsys' Design Compiler*** as the logic synthesis tool, and Cadence's Verilog-XL**** as the HDL simulator, and

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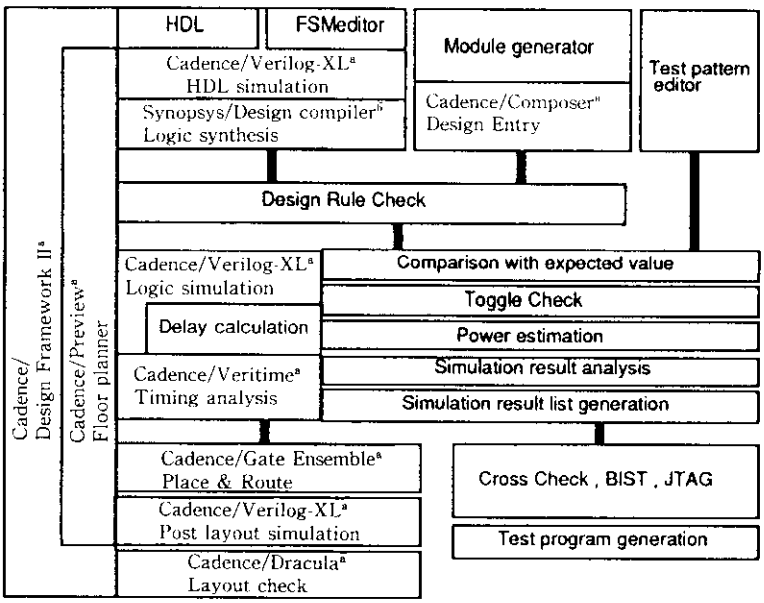
*** Design Compiler is the trademark of Synopsys, Inc.

**** Verilog-XL is the trademark of Cadence Design Systems, Inc.



[a]Trademark of Cadence Design Systems, Inc.
[b]Trademark of Synopsys, Inc.

Fig. 2 KSC CAD configuration

combining these elements with an interface tool between our original HDL design rule check and gate level design environment.

Top-down design describes functions in HDL, and verifies the HDL level function by means of HDL simulator. As a result, debugging in the early stage of design and, by extension, early detection of specification errors become possible. Function simulation, which is faster than gate level simulation, reduces function verification time. In addition, use of logic synthesis to automatically generate a gate level circuit from the HDL description of RTL (resister transfer level) contributes to a substantial reduction in logic circuit design time. Top-down design can shorten the development time required by a conventional gate-level design by 30%–50%.

4 CrossCheck Test Technology

Larger design sizes require more time to design a logic circuit, with an accompanying increase in the time needed to prepare a fault coverage test pattern. It has been common practice to manually prepare a fault coverage test pattern and verify it by means of a fault simulator. While this method requires a test pattern to discriminate faults in a circuit as well as a test pattern to propagate the discrimination results to the output pin of an LSI, an increase of LSI gate size makes it extremely difficult to prepare such test patterns. The Scan test method is available to solve this problem; however, it has many design restrictions and disadvantages such as penalties with respect to the speeds and areas of circuits.

An LSI using the CrossCheck test system includes, inside the chip, an exclusive test circuit provided with a function to check all inner nodes within a user circuit to be tested. As a result, the CrossCheck test system enables direct observation of faulty inner nodes, eliminates the need to propagate the fault to the output pin, and thus provides higher fault coverage by means of a simpler test pattern. In addition, CCL (CrossCheck Control Latch) technology makes it possible to write signals directly into flip-flops and latches in a circuit to

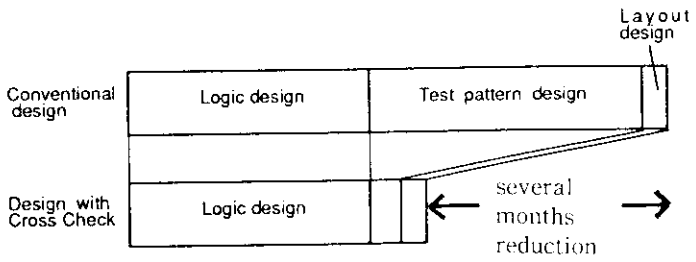


Fig. 3 Effectiveness by CrossCheck test method

automatically generate a test pattern even in the absence of a user pattern. Another important advantage of the CrossCheck system is the absence of penalty with respect to circuit speeds. **Figure 3** shows the effectiveness of the CrossCheck test system. In designing a circuit involving tens of thousands of gates, test pattern design time can be reduced by several months.

5 Application to Submicron Process

Conventional logic simulation uses driving capacity and output load capacity of a device for calculating delay. However, the advent of submicron processes involving larger errors between measured and simulation values calls for improved simulation accuracy. A simulation model has been developed which can calculate delay based on effects caused by varying input trip points (**Fig. 4**), and maintain errors with a measured value to 10% or less. Increasing micronization has increased the delay time resulting from routing load, rather than from logic gate delay time, with an accompanying increase in the probability of timing error in post layout simulation based on actual wiring length after automatic placement and routing. To solve this problem, a timing-driven layout has been realized in which the timing restriction is provided before automatic placement and routing to optimize the metal length in such a way as to satisfy the restriction. A floor plan has also been completed to make a hierarchical design of the layout.

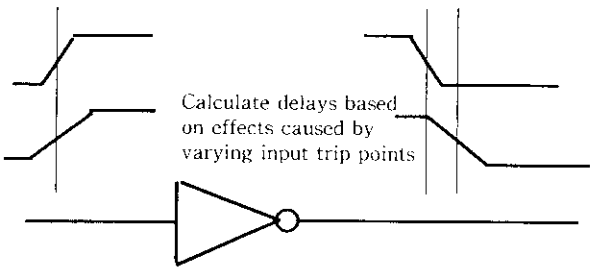


Fig. 4 Slew-rate dependent delay calculation

6 Original Tools of Kawasaki Steel Corp.

Design time has been reduced and operability improved by including, besides commercially available CAD tools, the following original Kawasaki Steel tools into the system:

(1) Generators
A memory generator for generating RAMs, 2 Port RAMs, and ROMs with any configuration and capacity to meet the need of a specific application, and a generator for generating ALUs and multipliers with any bit configuration have been developed. These generators, which work on the Cadence framework, offer automatic generation of a circuit drawing input symbol, logic simulator model, layout, and data sheet with a single operation.

(2) FSM Editor (Finite State Machine Editor)
A state transition diagram input editor has been developed capable of automatic generation of HDL, which can be logically synthesized, by inputting into the editor a state transition diagram without considering the HDL. The HDL thus generated can be input directly to a logic simulator for logic verification, and simultaneous input of the HDL into a logic synthesis tool provides automatic generation of a gate-level circuit, with a resultant reduction of logic design time.

(3) Design Rule Check
The design rule check is run to ensure that a logic circuit which has been designed presents no problem with respect to its driving capacity, its connections are free from defects, the number of gates to be used is contained in the die originally planned, and the next logic verification process can be undertaken.

(4) Simulation-Related Tools
The debug efficiency in logic verification and operability of the system have been improved by developing an expected value verification tool for automatic comparison of simulation results vs. expected values, simulation result list generation tool reflecting the results of expected value verification, toggle checking tool for simple verification of test pattern quality through checking of the toggle rate of a circuit prior to time-consuming faults simulation, and power consumption calculation tool for computing, from logic simulation results, the power consumption of a circuit for simple and reasonably accurate verification of the circuit. The simulation result analysis tool runs checks to ensure that the test pattern designed does not violate the rules of a tester and is free from noise that may cause malfunction of the circuit. These verification tools contribute to improved design quality and reduced design turnaround time.

7 ASIC Design Kits

There are increasing cases recently where ASIC users purchase CAD tools for structuring an ASIC design environment on their own. For users in possession of commercial tools, design kits for Cadence's Composer,***** Mentor's IDEA System,****** and Viewlogic's Workview System******* are available. A design kit consists of symbol and simulation libraries compatible with

***** Composer is the trademark of Cadence Design Systems, Inc.
****** IDEA-STATION is the trademark of Mentor Graphic Corporation
******* Workview is the trademark of Viewlogic Systems, Inc.

different CAD systems, and Kawasaki Steel's original tools, including a design rule check tool.

8 Concluding Remarks

A CAD system has been developed capable of designing, within a short time, large scale ASICs having gate counts of 100 000 or more. A state-of-the-art framework technology has been used to substantially improve the operability of the system. Top-down design has been put to practical use to substantially reduce verification time. Test pattern design becomes increasingly difficult with larger scale circuits involving tens of thousands of gates, but the CrossCheck test, which has been used to substantially cut design time for such large scale circuits, has succeeded in dramatically reducing test pattern design time from serveral months to several days. The user support program has been made more solid by strengthening support for commercial CADs including those of Cadence, Mentor, and Viewlogic. Future plans include structuring CADs capable of designing ASICs having hundreds of thousands to a million gates with a system-on-chip possibility.

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