New Products & Technologies

Image Compression and Decompression (JPEG) LSI Chip Set*

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1 Introduction

Increasing numbers of devices, including multimedia, are handling video signals, and since many of these devices involve digital processes, a strong demand has been created for digitization of video signals. Simple digitization of video signals, however, results in a substantial increase in the quantity of information, which is accompanied by an excessive load on process capability, memory capacity, and communication capacity. Thus, there is an increased need to reduce the number of data, and for continued efforts in this direction.

Video signal compression technology has shown remarkable growth recently, leading to the examination of various international standards. Kawasaki Steel has developed an LSI chip set conforming to the Joint Photographic Experts Group (JPEG) standard, an international standard for still pictures. The set consists of three chips: a DCT engine "KL5A71001," Huffman coders "KL5A71002," and a scan format converter "KL5A71101" for converting line scan into block scan.

2 Outline of JPEG Standard

The JPEG standard is an international standard for information compression involving still images (natural images). While the standard has many variations, including reversible compression and irreversible compression, along with their respective options, this paper describes a base line system, or a basic system.

In general, video signals contain a series of similar signals and redundant portions which cannot be recognized with human vision. This characteristic is used to reduce quantities of information for compression, in which the input signal is processed in a unit (block) of 64 pixels consisting of 8 lines of 8 pixels. On the block, DCT (discrete cosine transform), which transforms a signal from time base into frequency base, is performed to reduce the signal into frequency components. Video signals have concentrated energy in low frequency components, with relatively fewer signals in high frequency components. Next, a quantizer is used to reduce the high frequency components having relatively minor effect on human vision. The value of a quantizer table used then substantially determines the compression ratio and picture quality. This signal is further compressed by means of a Huffman encoder, which uses an externally set Huffman table to perform variable-length encoding. Encoding is completed by adding in the end a header matched to the JPEG format. Decompression is performed in reverse.

The compression ratio depends on the original copy and table used in quantization; the higher the compression ratio, the more conspicuous the deterioration of picture quality becomes. It is generally considered that no marked deterioration of picture quality occurs if the compression ratio is kept within the range of 1/10 to 1/20.

3 JPEG Compatible LSI Chip Set

Table 1 lists the main features of the JPEG compat-

Table 1 Features of JPEG chip set

- Baseline JPEG compatible compression and decompression
- Include JPEG framing markers
- Image formats: Gray-scale, RGB, CMYK (1:1:1:1), YUV (1:1:1), YUV (2:1:1), YUV (4:1:1)
- Supports up to 4 quantization tables and 2 sets of AC and DC Huffman tables
- Block-interleave format for pixel input and output
- Direct interface with IC memory card (JEIDA Version 4.1)
- Continuous throughput at 4 MHz data rate
- Can know the number of compressed data
- Can inhibit the compressed data output when reached specified value

* Originally published in *Kawasaki Steel Giho*, 26(1994)2, 100-102

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ible chip set (DCT engine, Huffman coders) developed by Kawasaki Steel.

As will be described later, the chip set includes such functions as to provide baseline JPEG compatible compression and decompression, direct interface with IC memory card (JEIDA Ver. 4.1), confirmation of the number of compressed data, and inhibition of the output of compressed data over and above a specified value.

Figure 1 is a block diagram for the chip set, of which the basic operation is described below.

Through the microprocessor interface (MPU interface), the mode of operation, number of pixels, and table to be used are set in the internal register to download both the quantization and Huffman tables. With commencement of compression, image data input from the pixel bus in block-interleave format is converted at the DCT engine into frequency components. After being quantized at the quantizer by the specified table, it is zigzag scanned (sequential scan, from low to high frequencies, of the frequency components in the block), then transmitted to the Huffman coders. After Huffman encoding in the Huffman encoder, it is output from the host bus with a header added. A memory card mode allows direct connection with any memory card conforming to JEIDA Ver.4.1. Direct access to the system register after compression can provide the number of compressed data. In addition, by setting in the register the maximum value of compressed data, it becomes possible to inhibit the output of compressed data over and above the preset value. Since, however, compression itself is continued, it is possible to find the number of final compressed data. This function is particularly effective for controlling the number of data.

4 Scan Format Converter

Compression by means of JPEG and MPEG (moving picture experts group) compatible DCTs is performed by processing data in a unit (block) of 64 pixels (8 pixels × 8 lines). Since ordinary image signals are scanned by one horizontal line, line scan must be converted into block scan prior to compression. **Figure 2** shows an image of the line scan-block scan conversion.

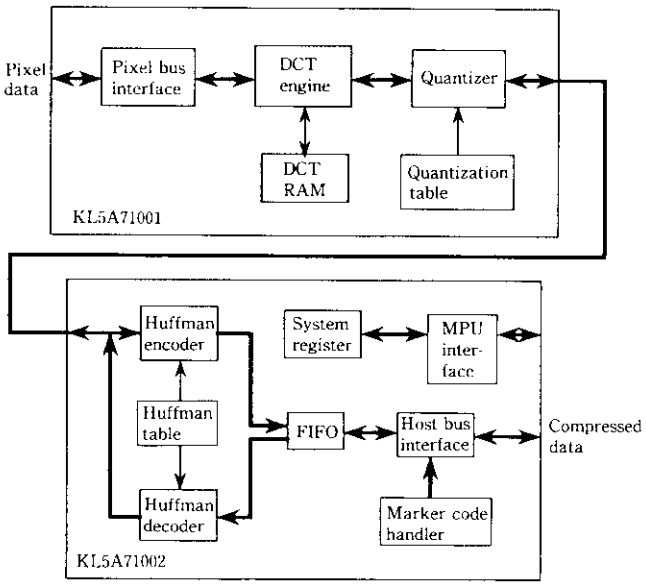

Fig. 1 Block diagram of the JPEG chip set

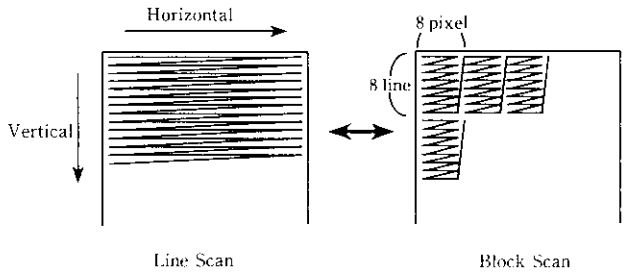

Fig. 2 Line scan-block scan conversion

Table 2 Features of scan format converter KL5A71101

- Conversion of raster-scan to block-scan and block-scan to raster-scan
- Block-scan format compatible with the "Minimum Coded Unit" structure of JPEG, MPEG and H.261
- Performs chrominance sampling rate conversion (YUV [4:2:2] -YUV [4:1:1])
- Supports CCIR 601 format
- Continuous throughput up to 27 MHz
- Performs elastic buffering (1-line buffer)
- JTAG (Joint Test Action Group) compliant

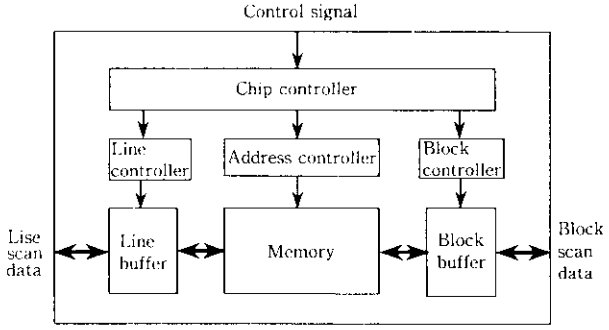

Fig. 3 Block diagram of the scan format converter

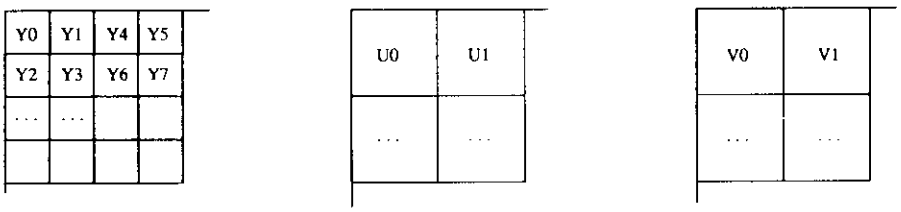

Fig. 4 Interleaved data ordering (YUV [4:2:0])

A circuit for this conversion normally consists of a number of chips including a line memory and its controller. We, however, have developed an LSI scan format converter which performs the same function in a chip with no external memory. Since it is a chip, the printed board space of the system and power consumption are reduced, and since no memory address and data bus are required, pattern design on the printed board is facilitated. **Table 2** lists the main features of the chip.

Figure 3 is a block diagram of the scan format converter, of which the basic operation is described below. The pixel bus, which has 24 bits, is used in 8, 16, or 24 bits in color formats. Input data passes through the buffer and is stored in the internal memory, where it is converted into block scan for output.

Sampling conversion can be made from YUV [2:1:1] into YUV [4:2:0], which is used in MPEG and others. While conversion from YUV [2:2:1] into YUV [4:2:0] outputs the average value of adjacent data, conversion from YUV [4:2:0] into YUV [2:1:1] shares the data between adjacent data. With this mode, it is possible to deal with the CCIR 601 format. **Figure 4** shows interleaved data ordering, in which one block each of color signals is output after four blocks of luminance signals are output.

Table 3 shows the maximum processable number of pixel data per line, in number per chip. These values can be increased through cascade connection.

Table 3 Maximum number of pixel data

Color format	Max. number of pixel data/line
YUV (2:1:1)	1024
YUV (2:1:1) sampling conversion	672
Monochrome	2048
RGB	680
CMYK	512
CCIR 601	720

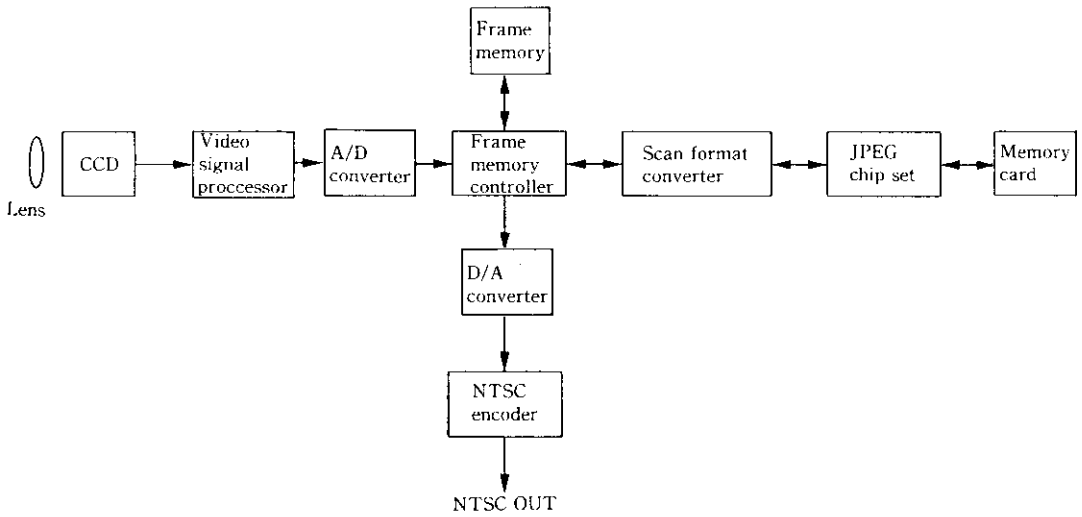

Fig. 5 Block diagram for the digital still camera

In addition, the possibility of using an internal memory as a buffer enables data output control. In addition, output can be temporarily suspended in the midst of continuous data input.

5 Applications

Using a JPEG compatible LSI chip set facilitates image compression conforming to the JPEG standard. Main applications include digital still cameras, picture files, still picture transmission devices, and image compression boards for personal computers. **Figure 5** shows a block diagram for a digital still camera. The application market for JPEG, which is not significant as of this writing, is gradually being prepared as standards are determined and semiconductor manufacturers start marketing their LSIs. It is expected that JPEG application products will be developed and commercialized in various fields in the future.

6 Concluding Remarks

A JPEG compatible LSI chip set has been developed as Kawasaki Steel's first product in the image compression area. Further development efforts will be continued in this promising area, including the development of general-purpose products to meet specific market needs and applications, as well as special-purpose products incorporating user logics. While the chip set just developed is limited to baseline applications, future plans include more advanced products adopting hierarchical coding and high-speed products compatible with moving picture images.

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