New Products & Technologies

General Purpose LSI Chip Sets for Image Processing —High Performance Two Dimensional Convolver, Median Filter, and Histogrammers*

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1 Introduction

The algorithms and system configurations required in image processing differ depending on the area of application. Where importance is attached to system flexibility, software processing is used; it is, however, limited in terms of processing speed. Processing speed can be increased through hardware only at the sacrifice of flexibility. On the other hand, both flexibility and high speed can be realized in a system built up with the LSIs employing highly generalized algorithms. From this standpoint, specific LSIs have been developed; "two dimensional convolvers," "median filter," and "histogrammers," each fabricated with the CMOS process. The following describes these LSIs.

2 Product Profiles

2.1 High Performance Two Dimensional Convolvers (HSP48908, 48901)

Two types of high performance two dimensional convolvers have been developed, which perform convolution on two dimensional signals with two dimensional impulse responses. Since both signals and impulse responses are discrete data in digital processing, convolution results in multiplication and additions. The range of additions should be finite to limit the circuit size to a realistic range, and a window should be set to specify the range of these additions. For the HSP48908 and 48901, the window size has been set to 3 × 3. Two dimensional convolution with this window size can be represented as follows:

$$\begin{aligned} P(m, n) = {} & A \cdot D(m+1, n+1) + B \cdot D(m, n+1) \\ & + C \cdot D(m-1, n+1) + D \cdot D(m+1, n) \\ & + E \cdot D(m, n) + F \cdot D(m-1, n) \\ & + G \cdot D(m+1, n-1) + H \cdot D(m, n-1) \\ & + I \cdot D(m-1, n-1) \quad \cdots\cdots\cdots\cdots (1) \end{aligned}$$

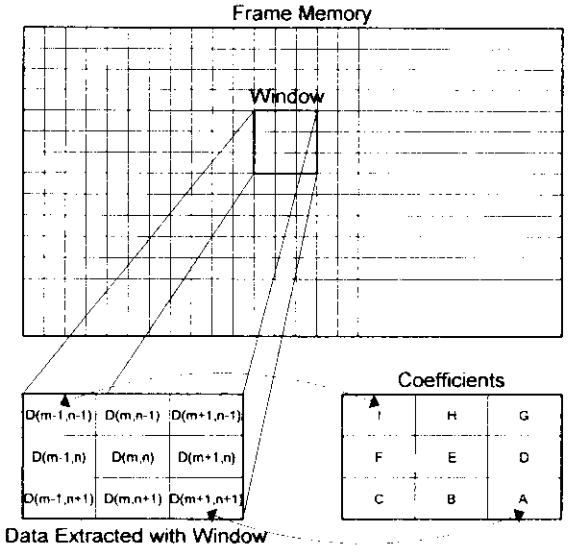

Fig. 1 Two dimensional convolution

where D(m, n) is digital data corresponding to pixels represented in coordinates (m, n) on the two dimensional space; A to I, window coefficients; and P(m, n), digital data to represent processed pixels. As shown in **Fig. 1**, a pixel given by coordinates (m, n) in a frame memory (a memory storing pixel data to form a frame of an image) and data to represent eight nearby pixels are extracted with a window, and each is multiplied by a different window coefficient to obtain the sum total of the products.

Figure 2 is a detailed block diagram showing the circuit used in the HSP48908 and 48901 for the operation of Eq. (1). Direct execution of the operation represented in this equation normally requires accessing the frame memory nine times to read out 9 data to obtain a single result. The HSP48908 and 48901 are each provided with a pipeline structure consisting of window registers and two line buffers for increased readout speed. To be specific, a frame memory is scanned for each clock, from left to right and top to bottom, to read out the data to be input into the register bank. D(n) is the data

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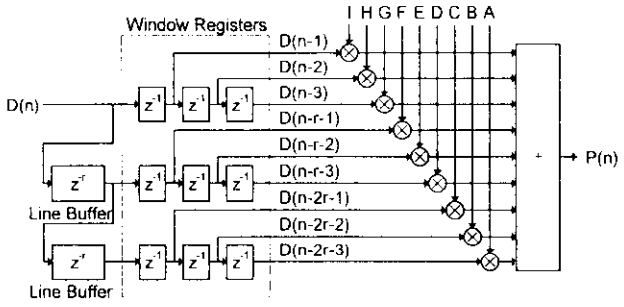

Fig. 2 Detailed block diagram of two dimensional convolver

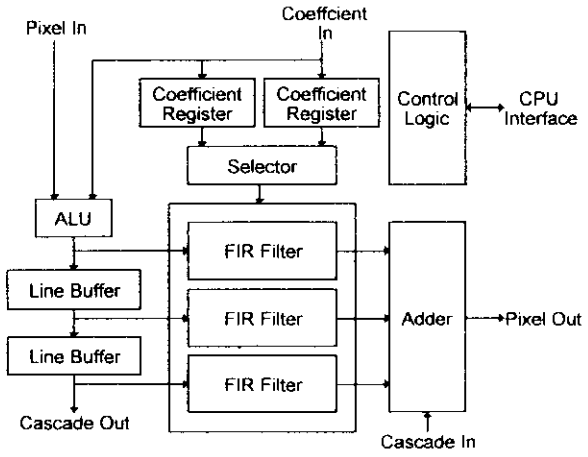

Fig. 3 Block diagram of HSP48908

to be read out at the nth access. When up to the third data on the third line is input, sufficient data is then accumulated in the window registers for one operation; thereafter, each time one pixel data is input, the content of the register is updated. In other words, a single access to a frame memory can provide the data necessary for one operation, enabling a reduction in overall processing time for large numbers of data. Data thus read out is processed by the circuit for multiplication and additions, and the result provided. The nine multipliers used in the circuit perform simultaneous multiplication of all nine terms indicated in Eq. (1).

Figure 3 shows a block diagram for the HSP48908 two dimensional convolver, in which window registers for one line and a circuit for multiplication and additions comprise FIR (finite impulse response) one dimensional filters, three of which are arranged via two line buffers to constitute a two dimensional convolver by obtaining a sum total with an adder in the final stage. The HSP48908 has built-in line buffers, while the HSP48901 requires external buffers.

By setting up coefficients in various ways, a two dimensional convolver can be applied to averaging process to reject random noises, the Laplacian process to extract the contour of an image, and others. For example, setting all coefficients A through I to 1 provides the sum total of data in the window, and dividing the result by 9 provides an averaging effect. Since data for a natural image generally exhibits a strong correlation within a local area, averaging the data, including noise, provides signals having a stronger mutual correlation and a resultant reduction in noise effect.

2.2 Median Filter (KL5A20015)

Random noise rejection through averaging by means of a two dimensional convolver results in an image with somewhat unclear contours. A median filter is used to obtain effective noise rejection without undue contour degradation.

As described above, image data shows a strong correlation in local areas, but luminance changes sharply in the contour area. Similarly, luminance also changes where noise exist. However, these two changes in luminance can be distinguished. If the luminance changes sharply in the contour area, data with a high correlation are lined up continuously before or after the change point, and when luminance changes sharply due to noise, many points of sharp changes are observed. It then becomes possible to reject noises by reading out data to represent an objective pixel and its nearby pixels, leaving behind only those data with a strong correlation. A median filter, which is means of leaving behind data with a strong correlation, selects the median of several pieces of data read out.

Figure 4 explains the operation of a median filter by showing how noises existing in one dimensional functions (function values a, b, c, . . .) are rejected. The functions form a gentle upward curve toward the right, with a point of sharp change along the line which represents a contour (change from c to d). It is to be assumed that data which should originally be g has become g′ because of noise. If data representing an objective points and point before and after this point are read out to

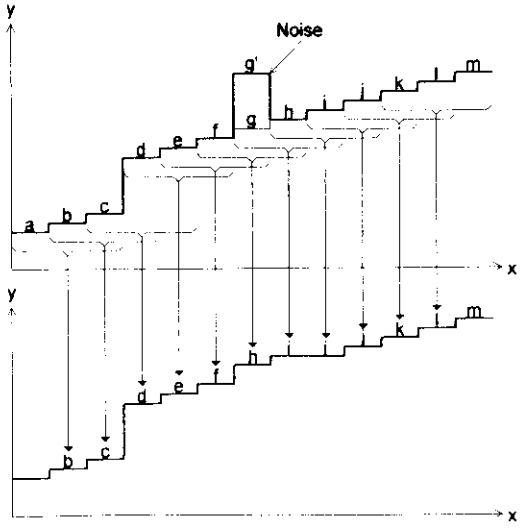

Fig. 4 Noise rejection by median filter

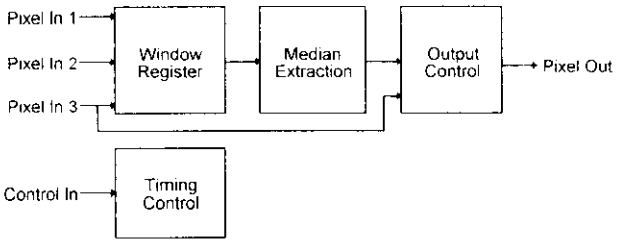

Fig. 5 Block diagram of KL5A20015

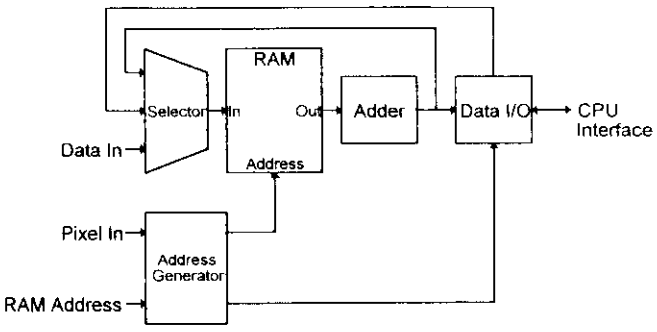

Fig. 6 Block diagram of HSP48410

select the median, the result is b, c, d, e, f, h, i, i, . . . , which means that the noises have been rejected with the original contour maintained.

An algorithm for selecting the median by sorting data according to value is a type of nonlinear processing. Since, however, data representing an objective pixel and its nearby pixels are read from a frame memory, a pipeline structure similar to that of a convolver can effectively increase processing speed. **Figure 5** represents a block diagram for the KL5A20015, in which details of a pipeline structure are omitted, and the line buffers are external.

2.3 Histogrammers (HSP48410, KL5A20016)

Two types of histogrammers have been developed; these are LSIs which count, according to luminance, the occurrences of data representing pixels to form a frame of picture. In general, a histogram of a natural image exhibits marked distribution of data in the dark and bright parts. Smoothing the distribution to allow data to average through the darkest to the brightest parts provides a clear image with strong contrast (with distinct differences in luminance). Contrast correction such as this is a typical application of histogrammers. In addition, extracting closed areas of each part of an image and generating a histogram of the data therein provides an area of each part. The histogrammers developed by the authors can also be applied to such image measuring tasks.

2.3.1 HSP48410 histogrammer

The HSP48410 can generate a histogram of an image consisting of 10-bit data with a size of up to $4\,096 \times 4\,096$ $(= 2^{12} \times 2^{12})$ pixels. In other words, a distribution of $16\,777\,216$ $(= 2^{24})$ pieces of data in total, capable of taking values from 0 to 1 023, can be obtained. This means that 1 024 24-bit counters are required, resulting in a circuit of excessive size. If, however, the individual data is read out from a frame memory and its attributes examined instead of trying to view the distribution of all data simultaneously, an incrementor, from among the elements forming a counter, can be shared to reduce the total gate counts of the circuit. It is also possible to reduce the circuit size by replacing a register bank, which is used to store count values, into a RAM. **Figure 6** is a block diagram of the HSP48410, in which image data read from a frame memory is input from Pixel In, used as an address to read data from the RAM, and then returned to the same address after 1 is added. This process, performed on the overall image data in a frame memory, generates a histogram in the RAM. In addition to histogramming, the HSP48410 can generate and store the cumulative distribution function. Other capabilities of the HSP48410 include data accumulation, a look-up table, delay memory, and an asynchronous interface with a host CPU. It is also provided with flash clear, which performs a single cycle reset on the previous histogram before processing of a new image.

2.3.2 KL5A20016 histogrammer

The KL5A20016, which is a histogrammer developed for such applications as use in industrial cameras as an input device, has a single capability of histogramming for frames up to 512×512 consisting of 8-bit data. It is provided with an automatic clear capability to automatically clear the previous histogram before processing of a new image.

3 Concluding Remarks

There are two approaches to improved performance in image processing LSIs: one is to micronize the process, and the other is to develop faster algorithms. The key to improved processing speed is the development of algorithms suited to hardware implementation. All LSIs described in this paper employ the pipeline structure or parallel process architecture for achieving high speed. Our future plans include the development of LSIs with multiple functions and higher flexibility, which will be effective in facilitating the construction of high performance image processing systems.

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