New Products & Technologies

Content Addressable ROM with a Variable Length Match Function–CAROM*

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1 Introduction

Semiconductor integration technology has made spectacular progress in recent years, giving birth to the general belief that in the 20th century memories with 1G bits will be commercialized to the point where they can be included in familiar portable devices. In other words, individuals will come to possess huge volumes of data. Conventional memories, in the meantime, are not well suited for accessing required data out of large numbers of data. Conventional memories, or address access type memories, do not read stored data directly; instead, they read data one by one sequentially through an address and make sure that it is the data of interest. As a result, the larger the number of data, the more difficult it becomes to address the required data. To solve this problem, a circuit technology which provides high-speed data retrieval without being restricted by the number of data has been developed[1] in the form of a 128 k bit high-speed content addressable ROM, or CAROM.

2 Features

The new CAROM LSI has the following three modes:

(1) ROM Mode
A mode in which data can be read by means of an address precisely as with standard memory devices.

(2) Data Retrieval Mode
A mode in which data, instead of an address, is input and compared with all stored data to check if there is any that matches requirements.

(3) Match Address Output Mode
A mode in which a location of stored data, which is found to match requirements in the data retrieval mode, is output as an address.

The cycle time for each mode is 120 ns (**Fig. 1**). **Figure 2** is a block diagram of the LSI, in which an external data bus as well as an internal word is con-

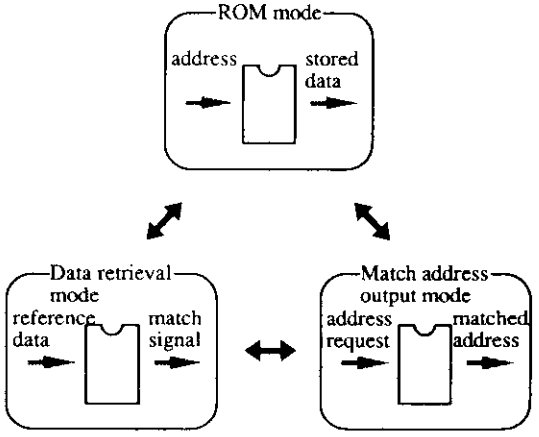

Fig. 1 Three operational modes of CAROM

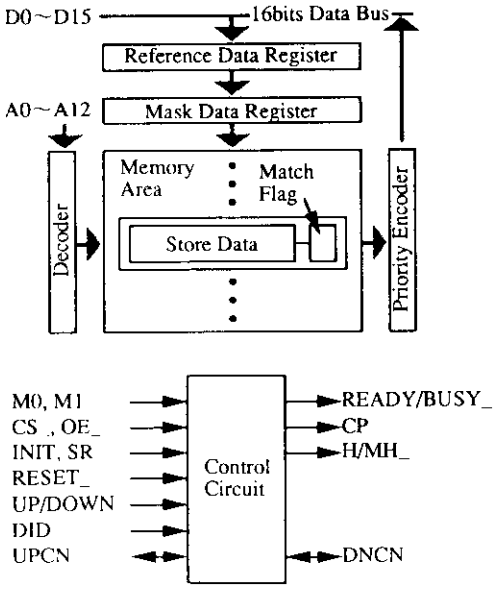

Fig. 2 Block diagram of CAROM

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figured in 16 bits, and a function is added to connect adjacent words. In addition, each word is provided with a match flag to indicate if it matches external data obtained in the data retrieval mode.

3 Operation

Figure 3 shows an example of operation. Consecutive addresses are loaded with X, Y, and 123. The first two are names called X and Y, and 123 to follow is a memory address in which reference data is stored.

In the retrieval mode, continuous search with two data X and Y completes a comparison and matching of all stored data in only 2 cycles and, in the end, a hit flag is set on the i-th Y word.

Then, in the address match mode, inputting a read pulse outputs the i address of the "Y" word. By incrementing the i address by one with the CPU and looking up the LSI set in the ROM mode with the $(i + 1)$ address, it becomes possible to output data "123." Using this data to look up other memories, data with respect to X and Y is provided instantaneously. Needless to say, it also becomes possible to use a "don't care" function in a bit unit at the time of retrieval and sequentially output multiple match addresses at the time of match address output.

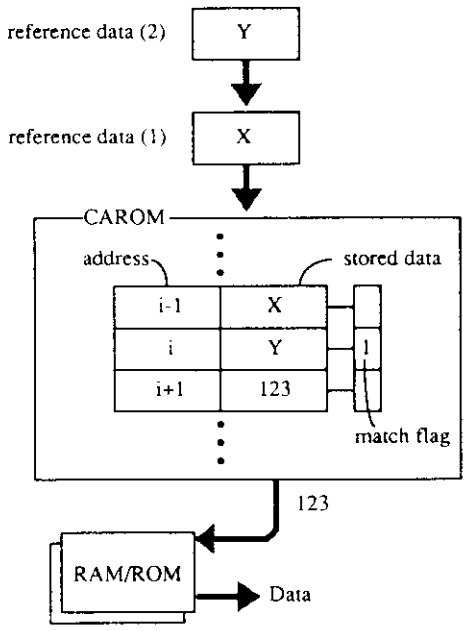

Fig. 3 Data flow chart of CAROM

4 Applications

High-speed content addressing of re-loadable memories is used for a high-speed addressing circuit in advanced microprocessors. In addition, a few other application examples have been reported.[2-4] However, the LSI reported here is the first high-speed LSI with large-scale integration for fixed data, which is also capable of handling data with variable length.

The CAROM, as a future fixed data storage element, is considered to have promising applications in the field of portable apparatus. The CAROM can also be applied to data flow control for handling data with variable length.

In addition, it is possible to use the CAROM, which is a re-loadable memory, as a table-processing LSI for high-speed data retrieval engines and high-speed networks, or as a hard macro for ASICs.

References

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