New Products & Technologies

0.8 μm CMOS High Density Gate Array "KZ2H"*

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1 Product Profile

To meet increasing demand for gate arrays with higher density, increased speed, and reduced power consumption, a KZ2H series of high density gate arrays has been developed. The series consists of 0.8 μm CMOS SOG (Sea of Gates) arrays utilizing the double layer wiring process. Each basic cell is composed of plural sizes of transistors efficiently suited to a wide variety of circuit configurations. The KZ2H series, while maintaining the quick TAT (turn around time) of the gate array, has realized density, speed, and power consumption comparable to those of standard cells. In particular, circuit density has been improved substantially to about double that of Kawasaki Steel's conventional 0.8 μm SOGs.

2 Development Rationale

Basic cells of conventional MOS gate arrays customarily have used, except for SRAM cells, uniform size of pMOS and nMOS transistors. In this case, there was an inevitable tendency to determine sizes taking the worst case circuit configuration, for example, in driving capability.

However, as indicated in **Fig. 1**, loads at most nets in actual circuits are relatively small and, in many cases, the transistor sizes of conventional gate arrays were too large for those nets, and meant nothing but a waste of silicon area.

On the other hand, with some types of macro cells, sequential circuits in particular, the circuit functions with elements of small driving capability. Even in this case, a large unified transistor size in conventional gate arrays wasted silicon area.

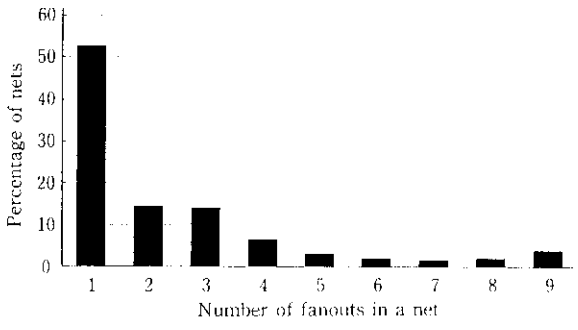

Fig. 1 Fanout distribution in a design

3 Product Characteristics

3.1 Architecture

In designing the KZ2H, load distribution at nets and the smallest possible size of transistors to be used in macro cells were analyzed statistically from existing designs, the most efficient transistor size and number of transistors required with particular sizes were determined without the restriction which would have been imposed by the conventional architecture with a unified transistor size, and the structure of the basic cell on the optimum arrangement of these transistors was established.

3.2 Performance Characteristics

The above architecture has realized simultaneous and substantial improvements of three major performance characteristics, density, speed, and power consumption, which were often considered contradictory requirements in the past. **Table 1** summarizes the above characteristics. **Table 2** compares the KZ2H with Kawasaki Steel's other ASCP (application specific custom products) families. The gate utilization used in the density calculation for KZ2H is 40%.

The circuit density, in particular, has been almost doubled to that of the KG2H, an SOG of conventional architecture (with a built-in CrossCheck*** test function), which is higher than that of Kawasaki Steel's standard cell, the KS2H (also with a built-in CrossCheck test function). Even after discounting minor areal over-

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*** CrossCheck is the registered trademark of CrossCheck Technology, Inc.

Table 1 Specifications of KZ2H family

Process	0.8μm CMOS double layer metal
Delay time[a]	0.27 ns
Max. usable gates	460 K gates
Voltage	5 V±10% 3.3 V±0.3 V 3 V±10%
Power dissipation[b]	3.1 μW/MHz/gate

[a] Power 2NAND, FO=2, Al=2mm
[b] 2NAND, FO=2, Al=0.34mm

Table 2 Comparison between KZ2H and other ASCP families

(Relative value, %)

	SOG		Standard cell
	KZ2H	KG2H	KS2H
Density	100	~50	~80
Speed	100	~70	~90
Power	100	~160	~110
CrossCheck		available	available

head associated with the KG2H and KS2H resulting from inclusion of the CrossCheck test function, the density improvement with the KZ2H is still substantial.

In operating speed and power consumption as well, the KZ2H is superior to conventional SOGs and standard cells. While in Table 2 the same metal length has been assumed for both KZ2H and the conventional ASCP families, the actual operating speed and power consumption after making the layout are expected to be further improved because, with the KZ2H, the wiring length is actually shortened due to the reduction in the chip area.

As a result, the KZ2H series makes it possible, while maintaining the same short TAT as a gate array, to design custom circuits with efficiency equivalent to those of standard cells. With respect to circuit density in particular, the core area can be only about 50% of that of Kawasaki Steel's conventional gate array, and it becomes possible to accommodate in the same die a circuit with twice the gate count as that of a conventional one. In addition, there are other advantages such as an operating frequency higher than those of conventional gate arrays, or reduced power consumption. The latter can limit a rise in junction temperature and makes it possible to mount a die with a more complex circuit in a plastic package.

As can be seen from the foregoing, the KZ2H not only covers the application area of conventional gate arrays, but also is an optimal product for high-volume and high-end designs. Specifically, the characteristics of the KZ2H can fully be utilized where cost and performance equivalent to those of standard cells are required while maintaining a short TAT to ensure a satisfactory product life cycle, or where substantial cost reduction is sought with the current packages for gate arrays.

4 Product Contents

4.1 Die Line-up

Table 3 lists a standard KZ2H die line-up. The maximum number of usable gates reaches as many as 460 000. In addition, the KZ2H series provides the flexibility to make custom dies with sizes in accordance with customers' requirements in such a way as to make the most effective use of its high density characteristics. To

Table 3 Example of KZ2H die line-up

Die code	No. of available gates	No. of usable gates	No. of pads
KZ2H002	22 382	8 953	68
KZ2H005	48 238	19 295	100
KZ2H007	69 380	27 752	120
KZ2H010	99 806	39 922	144
KZ2H016	155 790	62 316	180
KZ2H021	207 914	83 166	208
KZ2H038	376 430	150 572	280
KZ2H054	541 825	216 730	336
KZ2H080	798 610	319 444	408
KZ2H115	1 154 098	461 639	488

facilitate this arrangement, tools such as a base array compiler are available for the KZ2H.

4.2 Libraries

For the KZ2H series, about 350 macro cells with approximately 150 functions are available. One function is provided with up to four levels of driving strength, so that a trade-off can be selected for each cell with respect to its area and speed.

In addition, the KZ2H library provides good matching to logic synthesis, which is becoming widely accepted in the industry. Specifically, the input polarity of each macro cell has been provided with a variety of inverted polarities so that logic synthesis software can make an efficient polarity selection to facilitate circuit optimization in area and speed.

With respect to mega cells for CPUs and their peripheral circuits, the same assortment as that for the KG2H is available.

4.3 SRAMs

Table 4 shows SRAMs available for the KZ2H series. Two are asynchronous SRAMs with the main emphasis on high speed, and one is synchronous, with a view to reducing power consumption mainly at low to intermediate speeds.

4.4 CAD Systems

The CAD system is arranged based on popular and readily available commercial tools, to which tools specific to the KZ2H series have been added.

Table 4 Specifications of KZ2H SRAM's

	1-port asynchronous SRAM	2-port asynchronous SRAM	1-port synchronous SRAM
No. of R/W ports	1 R/W	2 R/W	1 R/W
Max. No. of bits	18 K	9 K	36 K
Word range	64～2 K	32～1 K	64～2 K
Bit range	1～36	1～36	1～36
T_{aa}(ns)	5.5[a]	5.9[a]	7[b]
T_{wc}(ns)	3.6[a]	4.3[a]	11[b]

[a] For 32 bits/word×512words
[b] For 9 bits/word×2 084words

Commercial tools include Composer (Cadence Design Systems, Inc.) for the schematic entry, Design Compiler (Synopsys Inc.) for logic synthesis, Verilog (Cadence Design Systems, Inc.) for simulation, and Gate Ensemble (Cadence Design Systems, Inc.) for layout.

Tools added to the above include SiArc's Design Advisor (design rule verification tool), Delay Annotator (delay information generation tool for Verilog), and SRAM Compiler (SRAM generator).

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