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Munetaka Koda, Junichi Kawaguchi, Yoshikatsu Shida

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Improving Gate Oxide Integrity in p⁺pMOS Devices by Using Large Grain Polysilicon Gate*

Munetaka Koda
Senior Researcher, LSI Research Center, High-Technology Res. Labs., Technical Res. Div.

Junichi Kawaguchi
LSI Research Center, High-Technology Res. Labs., Technical Res. Div.

Yoshikatsu Shida
LSI Research Center, High-Technology Res. Labs., Technical Res. Div.

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1 Introduction

As CMOS technology is scaled down to dimensions of below 0.5 μm, it is necessary to use n^+ polysilicon gates on nMOSFET and p^+ polysilicon gates on pMOSFET so that both devices act as surface channel transistors with proper short-channel characteristics.[1,2] The simplest process for fabricating such dual gate CMOS devices is to dope the polysilicon gate after they are patterned with the same implants as the n^+ and p^+ source-drain implants.[3] This not only minimizes the number of masks but also avoids the problem of different n^+ and p^+ polysilicon etch rates when doping is done before patterning. However, many problems with p^+pMOSFET were reported. When BF_2 is used for gate-S/D co-ion implantation, the fluorine enhances boron penetration through the gate oxide into the channel region.[4] This boron penetration results in a positive shift in the p-channel threshold voltage. Fluorine reduced the dielectric constant of oxide and decreased gate oxide capacitance.[5,6] Furthermore, we have found that gate oxide in a low BF_2-implanted polysilicon gate capacitor showed low-voltage breakdown.[7] In this paper, the problems with p^+pMOSFET are shown to be related to the grain size and structure of polysilicon. Thus, problems such as gate oxide deterioration, boron penetration, and low oxide capacitance can be solved by using large grain polysilicon.

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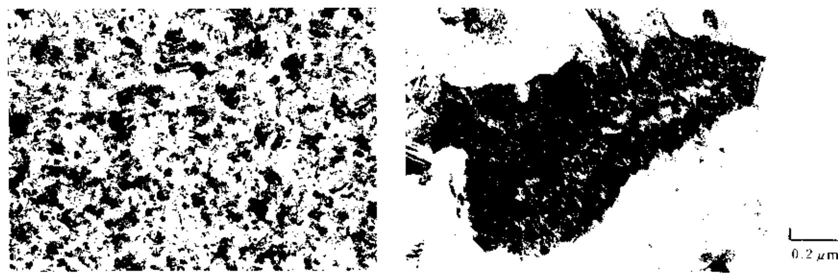
2 Experimental

The effect of the grain size and structure of polysilicon on gate oxide integrity, boron penetration, and gate oxide capacitance was investigated. The MOS capacitors used in the study were fabricated as follows: A scarified oxide was stripped and RCA-cleaning was performed immediately prior to growth of the gate oxide on a (100) n-type silicon substrate. For the gate oxide, 8 nm silicon dioxide and nitrided oxides were used. Nitridation of the silicon dioxide was performed in N_2O. Immediately after oxide growth, a 150 nm undoped silicon film was deposited, and the grain size and structure of this film were controlled by changing the film-formation conditions as shown in **Table 1**. An amorphous silicon film was deposited at 480°C by using Si_2H_6 gas and crystallized at 650°C for 5 h to form large grain polysilicon. Planar TEM photographs of conventional and large grain polysilicon samples are shown in **Photo 1**. The

Table 1 Conditions for polysilicon film formation

	CVD		Annealing
	Source gas	Temperature	
Conventional polysilicon	SiH_4	620°C	—
Large-grain polysilicon	Si_2H_6	480°C	650°C for 5 h in N_2



(a) Conventional polysilicon (b) Large-grain polysilicon

Photo 1 TEM plan-views of the polysilicon film

average grain sizes of conventional polysilicon (small grain) and large grain polysilicon are on the order of 0.05 μm and 1.0 μm, respectively. The undoped polysilicon was then oxidized (4 nm in thickness) and implanted with BF_2. After LTO and BPSG had been deposited, the samples were annealed at 900°C for 30 min in N_2 to activate the dopant.

A time-zero dielectric breakdown (TZDB) test was performed on 108 capacitors with an active area of 4 mm^2. The gate oxide breakdown voltage is defined as the voltage required for a current density of 32 mA/cm^2 to flow through the capacitor. A constant current time-dependent dielectric breakdown (TDDB) test was also performed on 108 capacitors with an area of 1 mm^2. Capacitance measurement was performed on a MOS capacitor with an active area of 0.25 mm^2 to study boron penetration and decrease of gate oxide capacitance.

3 Results and Discussion

3.1 Gate Oxide Quality

Figure 1 shows breakdown histograms for conventional and large grain polysilicon gate capacitors with the 8 nm nitrided oxide. This figure indicates that the gate oxide quality of the capacitor with conventional polysilicon was inferior to that with large grain polysilicon. In 26% of capacitors with a conventional polysilicon gate, the gate oxide shows low-voltage (below 2 V) breakdown. The oxide defect density was calculated to be as high as 7.5 cm^{-2}. This inferior quality was improved by using large grain polysilicon. The number of gate oxide breakdowns at low voltage decreased, and the gate oxide in almost all capacitors showed breakdown at high-voltage. In this case, the defect density was as low as 0.3 cm^{-2}.

It is believed that the bad gate oxide quality in conventional polysilicon is brought about not by any degradation of oxide quality, but by the generation of weak spots in the gate oxide. **Photo 2** shows dark field TEM micrographs of the small grain and large grain polysilicons. The direction of the electron beam was parallel to the interface between the polysilicon and gate oxide, which coincides with the [101] direction of the silicon substrate. The interface between the polysilicon and gate oxide is as smooth as that between the gate oxide and silicon substrate in large grain polysilicon gate MOS capacitor. On the contrary, gate oxide thinning occurred in conventional polysilicon gate MOS capacitors. Low voltage breakdown in conventional polysilicon gate MOS capacitors could occur at the points. The mechanism of this phenomena can be explained as follows: When the polysilicon films were oxidized and annealed, a compressive stress was generated in the polysilicon film by expansion of polysilicon grain boundary. Oxidizing and annealing process resulted in a Raman peak

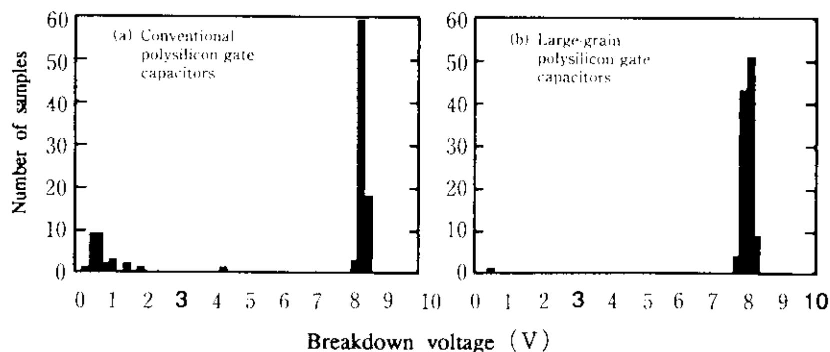
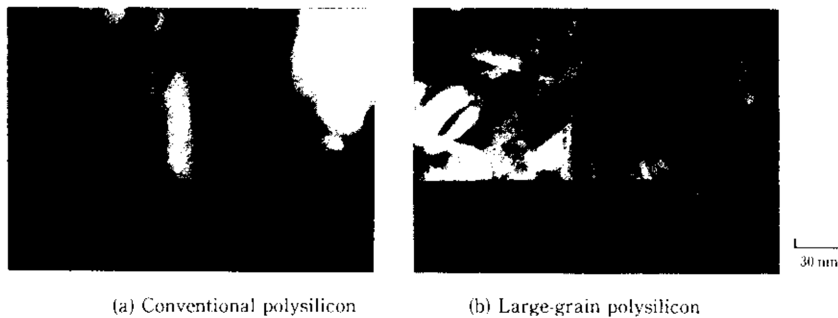
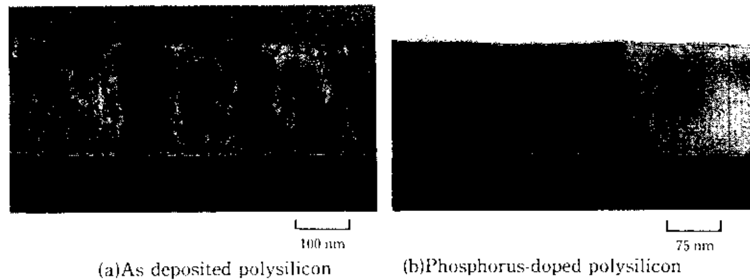


Fig. 1 Histograms for the time-zero dielectric breakdown voltage of gate oxide capacitors with 8 nm nitrided oxide



(a) Conventional polysilicon (b) Large-grain polysilicon

Photo 2 Dark-field TEM micrographs



(a)As deposited polysilicon (b)Phosphorus-doped polysilicon

Photo 3 Cross-sectional TEM micrographs of the polysilicon films

shift to a higher wave number by 1.0 cm^{-1}, which corresponds to a stress of 2.5×10^9 dyn/cm^2(2.5 MPa). Wedge-shaped grains were found clinging to the gate oxide in the polysilicon. The grains were pushed into the gate oxide by the compressive stress during oxidization and annealing.

This was a unique phenomenon observed in BF_2 implanted polysilicon gate pMOS devices. Boron has no effect on the enhancement of the grain growth during heat treatment, which is contrary to the results with phosphorus and arsenic doped polysilicon.[8] Wedge-shaped grains, which existed in as-deposited polysilicon, did not disappear during heat treatment because of insufficient grain growth.

On the contrary, grain-growth occur easily and wedge-shaped grains disappear in phosphorus and arsenic doped polysilicon. **Photo 3** shows TEM micrographs of the phosphorus doped polysilicon. Large grain polysilicon had no wedge-shaped grains under a deposited condition similar to that for phosphorus doped polysilicon, and good gate oxide quality was obtained.

Figures 2 and **3** show the cumulative failure vs. charges to breakdown (Q_{bd}) in capacitors with nitrided oxide and silicon dioxide, respectively. In Fig. 2, the gate oxide in 30% of the capacitors with a conventional polysilicon gate shows breakdown immediately after a voltage was applied to the capacitor. On the other hand, the large grain polysilicon gate capacitors showed superior gate oxide quality in the random failure region, which explains the results presented in Fig. 2. A similar result was also obtained for the 8 nm silicon dioxide

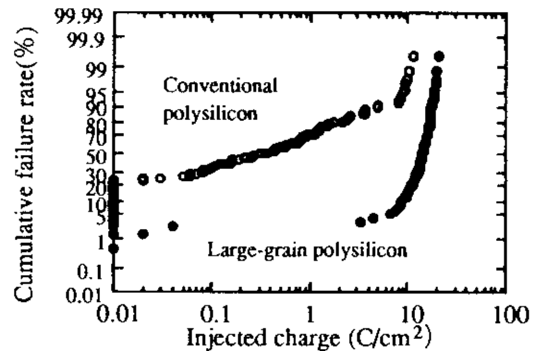


Fig. 2 Cumulative failure *vs* injected charge to breakdown for conventional and large-grain polysilicon gate capacitors with 8 nm nitrided oxide

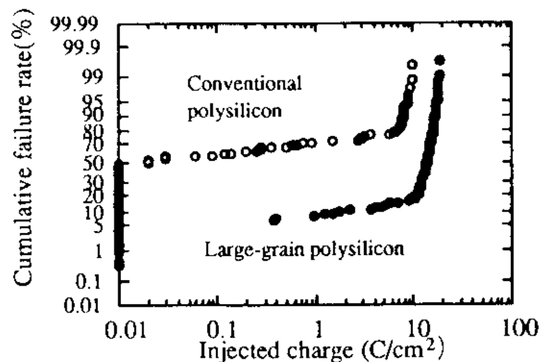


Fig. 3 Cumulative failure *vs* injected charge to breakdown for conventional and large-grain polysilicon gate capacitors with 8 nm wet oxide

capacitors as shown in Fig. 3. Q_{bd} at 50% failure with the large grain polysilicon gate capacitor is twice as large as that in the conventional polysilicon type. The use of the large grain polysilicon gate lowered the gate oxide defect density and improved the gate oxide reliability.

3.2 Boron Penetration through Gate Oxide

Figure 4 shows the relationship BF_2 dosage and flatband voltage for the capacitors with 8 nm wet oxide. BF_2 ions were implanted at the dosage of $2 \times 10^{15}/cm^2$ and annealed at 900°C for 30 min. The flatband voltage of the capacitor without boron penetration was measured as 0.95 V from the work function difference between the silicon substrate and p^+ polysilicon. The flatband voltage of the large grain polysilicon gate capacitor was 0.95 V at a BF_2 dosage of $2 \times 10^{15}/cm^2$, which means boron had not penetrated. However, the flatband voltage of the conventional polysilicon gate MOS capacitor was 1.55 V at the same dosage of BF_2, which means boron had penetrated. The large grain polysilicon gate suppressed boron penetration. The flatband voltage of the large grain polysilicon gate capacitor was 1.05 V and 1.02 V at dosages of 5×10^{15} and $1 \times 10^{16}/cm^2$, respectively. The flatband voltage increase from 0.95 V could be not due to boron penetration but due to a negative charge generated in the gate oxide.

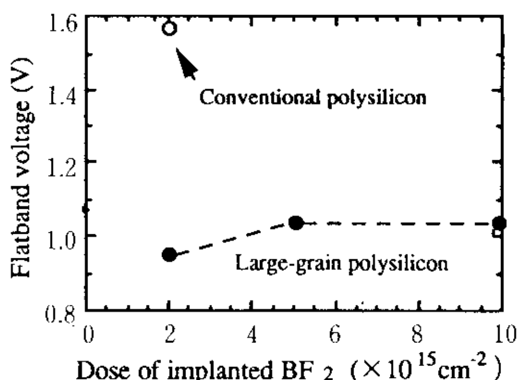


Fig. 4 Flatband voltage as a function of BF_2 dosage for conventional and large-grain polysilicon gate capacitors with 8 nm wet oxide

3.3 Gate Oxide Capacitance and Inversion Capacitance Decrease

Figure 5 shows the relationship between gate oxide capacitance (C_{ox}) at a gate voltage of 3.3 V and BF_2 dosage. A heavy phosphorus doped polysilicon gate MOS capacitor, whose capacitance was 1 nF, was used as a reference. The capacitance of the large grain polysilicon gate was 980 pF, which was 2% smaller than the reference capacitance. In contrast, the capacitance of a conventional polysilicon gate was 12% smaller than the reference capacitance. The large capacitance decrease in

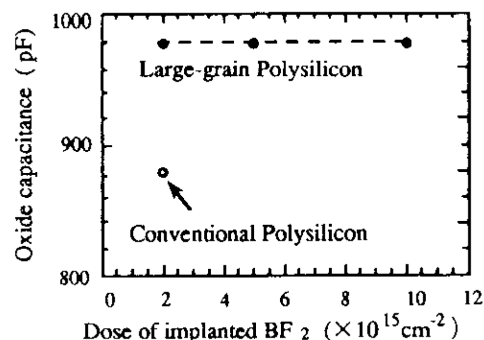


Fig. 5 The effect of implant dosage of BF_2 on oxide capacitance for conventional and large-grain polysilicon with 8 nm wet oxide

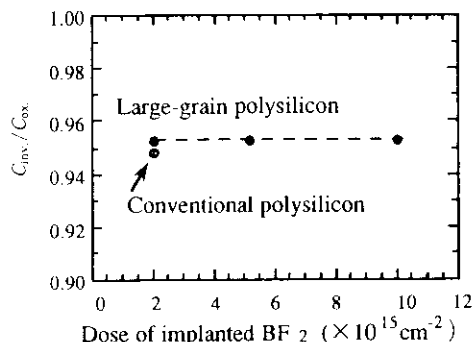


Fig. 6 C_{inv}/C_{ox} as a function of BF_2 dosage for conventional and large-grain polysilcon gate capacitors with 8 nm wet oxide

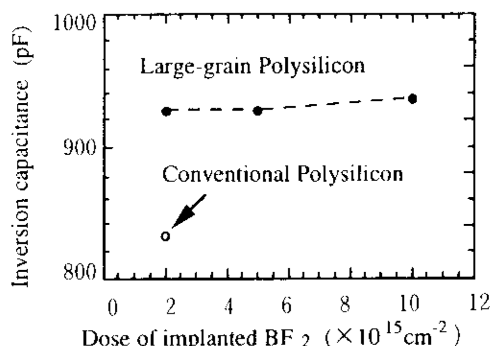


Fig. 7 The effect of dosage of BF_2 on inversion capacitance for conventional and large-grain polysilicon with 8 nm wet oxide

conventional polysilicon gate MOS capacitors occurs due to a dielectric constant decrease or additional gate oxide growth at a high level of fluorine.[5,6] **Figures 6 and 7** shows the BF_2 dosage dependence of C_{inv}/C_{ox}, and that of C_{inv}, respectively. C_{inv} means the capacitance of an MOS capacitor at the inversion condition from quasi-

static CV measurement, and C_{inv}/C_{ox} is a parameter which is related to the carrier concentration in the polysilicon. C_{inv}/C_{ox} shows little difference in the two types of polysilicons. However, the C_{inv} of large grain polysilicon gate MOS capacitors differs from that of conventional polysilicon gate MOS capacitors. Large grain polysilicon gate suppress the decrease in gate oxide capacitance and inversion capacitance.

4 Conclusions

The effect of polysilicon grain size and morphology on gate oxide integrity, boron penetration, and gate oxide capacitance in p^+pMOS devices was investigated, with the following results:

(1) Conventional polysilicon (0.05 μm) degraded gate oxide integrity.
(2) The use of large grain (1.0 μm) polysilicon gates solved the problem of poor gate oxide quality.
(3) The low gate oxide quality of conventional polysilicon gate MOS capacitors is possibly attributable to gate oxide thinning, which can be suppressed by the use of a large grain polysilicon gate.
(4) Large grain polysilicon prevented boron diffusion through the gate oxide.
(5) Large grain polysilicon gates suppressed gate oxide capacitance decreases.

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