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0.8-micron CMOS ASCPs

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The 0.8μm double layer metal ASCPs (Application Specific Customized Products such as gate array, embedded array and standard cell) have been developed. All products have achieved one of the highest raw gate count and the least power in the industry. The circuit on the chip has become larger, and the difficulty of the test has increased dramatically. Considering this situation, Kawasaki Steel has decided to introduce the CrossCheck CX-ArrayTest technology into all of the 0.8-micron ASIC products. CrossCheck CX-ArrayTest features the ATPG (automatic test pattern generation) even for the asynchronous circuit. Kawasaki Steel also has developed the BIST circuit for memory testing and JTAG compatible boundary scan circuit for board level testing. For very large system design, the memory or other large functions are indispensable. The 0.8μm ASCPs support the on-chip memory compiler and the originally developed 8-bit CPU core which is compatible with Zilog Z80.

The body can be viewed from the next page.

0.8-micron CMOS ASCPs*

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1 Introduction

While applications having tens of thousands to hundreds of thousands of gates are no longer uncommon, integrating a large scale circuit on a single chip LSI involves a number of problems such as (1) increased power consumption and (2) more difficult test methods with increasing gate count. **Figure 1**, showing the relation between power consumption and gate count,[1] indicates that power consumption becomes more than about 1 W when the gate count exceeds 10 000. Circuits that can be sealed into inexpensive plastic packages are normally limited to those with power consumptions of up to about 1 W. Anything above this level must use a heat sink or ceramic package with low thermal resistance. It is therefore obvious that reducing power consumption is important from the standpoint of reducing cost.

Furthermore, the larger the circuit, the more difficult the pattern generation becomes. While increasing gate count results in an accompanying increase in circuit nodes to be tested, the number of input output signal pins required to control and monitor the circuit nodes for detecting faults is limited to about 200. **Figure 2** shows the relation between gate counts and test pattern

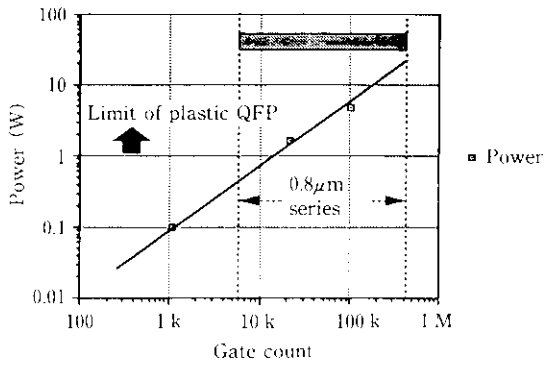

Fig. 1 Example of power increase *vs* gate count

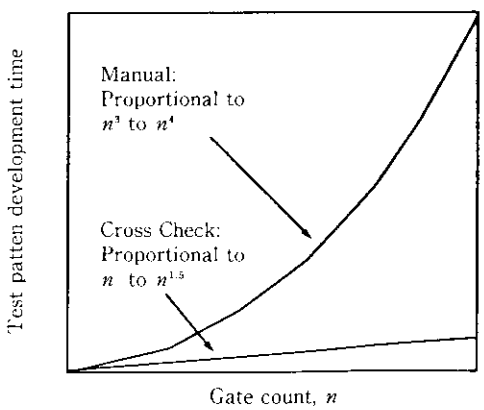

Fig. 2 Relationship between gate count and test pattern development time

* Originally published in *Kawasaki Steel Giho*, **26**(1992)2, 60–64

development time, from which it can be seen that the test pattern development time increases proportionally to the third and fourth power of any gate count.[2] From the foregoing, it is obvious that unless test pattern generation is somehow automated and facilitated, "time-to-market" requirement will present serious problems.

This report describes Kawasaki Steel's ASCPs (application specific standard products) developed with the main emphasis on reduced power consumption and improved test facility.

2 Products and Basic Specifications

Table 1 summarizes the basic specifications of the gate arrays "KG2H series" and standard cells "KS2H series" developed with Kawasaki Steel's 0.8 μm double layer wiring process technology. In the table, embedded arrays "KE2H series," which are identical with the KG2H except for memory and macro functions, are shown in the same column as the KG2H. The KG2H and KE2H series have about 2.4 times as many available gates (on the basis of 4 Trs. = 1 gate) as Kawasaki Steel's 1.0 μm series (KL9H and KE9H), about half the power consumption, and a delay time improved by 33%. The KS2H series has also realized about 2.4 times as many available gates and about half the power consumption of Kawasaki Steel's 1.0 μm (KS9H) series.

Both the KG2H and KE2H series rely on the CX-Array/Test of CrossCheck Technology Inc. to facilitate tests, dramatically reducing test pattern development time. In addition, the KS2H series provides the first standard cell products in the world to include the CrossCheck test circuits, embodying an ASCP product line with particular emphasis on improved test facility.

Table 1 Specifications of 0.8 μm ASCP

Product	Gate array/ embedded array		Standard cell	
	KG2H/ KE2H series	KL9H/ KE9H series	KS2H series	KS9H series
Design rule	0.8 μm	1.0 μm	0.8 μm	1.0 μm
Available gates	171 k gates	72.2 k gates	257 k gates	107 k gates
Tpd (f.o.2. wire 2mm)	0.4 ns	0.6 ns	0.3 ns	0.7 ns
Cell power	5 μW/ MHz	10 μW/ MHz	3.3 μW/ MHz	5.6 μW/ MHz
Cell utilization	~60%	~40%		
Test method	CrossCheck	Normal	CrossCheck	Normal

Tpd : propagation delay (f.o., 2; wire, 2 mm)

3 Technology of 0.8-μm ASCPs

3.1 Process Technology

Table 2 shows features of Kawasaki Steel's 0.8 μm process technology. As can be seen from the table, metal pitches have been improved substantially by reducing metal widths and contact sizes. **Figure 3** shows the metal pitch vs. process technology reported in academic societies,[3,4] and clearly indicates the smallness of the metal pitches realized with Kawasaki Steel's 0.8 μm process technology.

Table 2 Key process parameters

Parameters	Nominal values
Channel length (P/N)	0.8 μm/0.8 μm
Device Vt. (P/N)	0.7 V/−0.7 V
Gate oxide thickness	15 nm
1st metal pitch (width+space)	2.4 μm
2nd metal pitch (width+space)	2.4 μm
Contact size	0.8 μm
Via size	0.8 μm

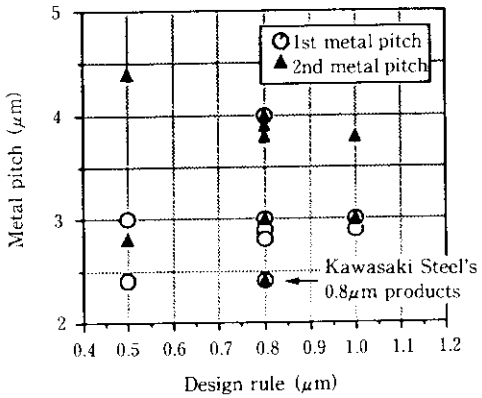

Fig. 3 Reported metal pitch *vs* design rule

3.2 Core Cells

Core cells embodying lower power consumption and higher density have been developed. To reduce power consumption, transistor size has been reduced to curb input capacity and totempole current. To increase density, wiring efficiency has been improved by means of a core cell structure which allows larger wiring space. In addition, the KG2H series is designed to allow one bit of single port RAM to be configured with one cell so that the memories essential in large scale ASICs can be realized efficiently. A core cell consists of a total of nine transistors, including very small ones (sense transistors), to form a CrossCheck test circuit.

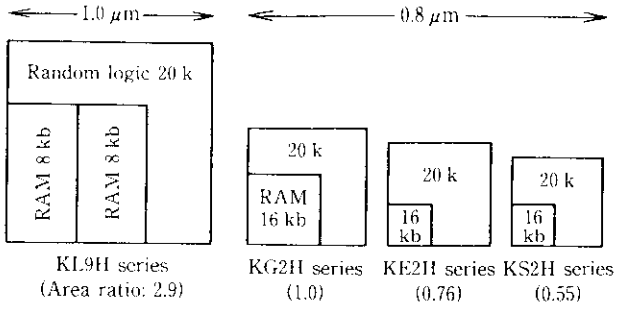

Fig. 4 Area comparison between Kawasaki Steel's ASCPs

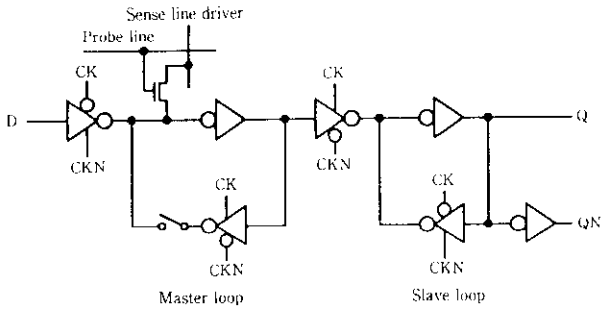

Fig. 6 Cross control latch (CCL) structure

For the KS2H series, the optimal area and performance have been realized through optimization of transistor size and removal of unnecessary diffusion layers. **Figure 4** is an areal comparison of the KL9H series (1.0 μm). KG2H series, KE2H series, and KS2H series when, as an example, a circuit consisting of a random circuit with 20 k gates (on the basis of 4 transistors = 1 gate) and single port RAM with 16 k bits is structured (without input and output buffers). The figure shows relative ratios, with the KG2H series as 1.

3.3 CrossCheck Technology

Figure 5 is an image drawing of an LSI including CrossCheck test circuits, in which matrix sense and probe lines are arranged on a chip with a sense transistor provided on each node. A library cell is designed by adding a sense transistor to each output terminal and inner node, which are subsequently included in a matrix test circuit at the time of automatic placement and wiring. At the time of testing, sense and probe lines are driven by probe line drivers and a control circuit, or test electronics, for sequential reading of voltage information of the circuit by means of a sense line receiver.

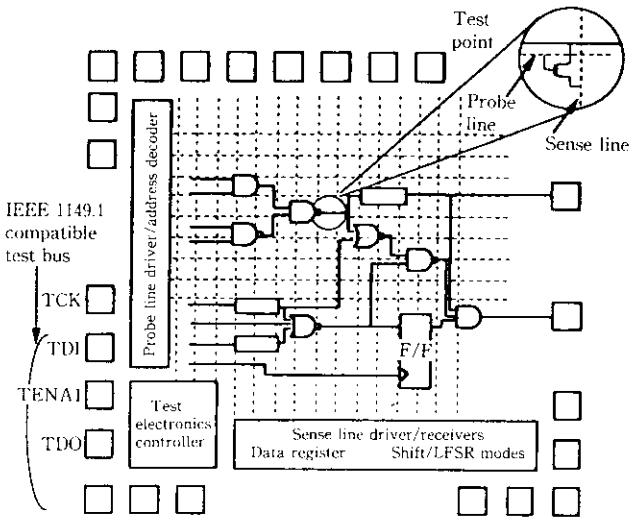

Fig. 5 CrossCheck test circuits

The voltage information, which contains large numbers of data as it is read, is compressed by an LFSR (linear feedback shift register) circuit and output as a signature. The quality of the signature thus obtained is determined by comparing it with a fair signature obtained by logical simulation. The ability to read out voltage information at all points in a circuit provides excellent observability (a measure to represent testability).

While conventional test methods were able to read values only at the output pin of an LSI, the CrossCheck test allows them to be read them at all matrix nodes of sense and probe lines. The CX-ArrayTest also allows values to be written from test electronics, through sense lines, to sequential circuits such as flip-flops having a structure called CCL (cross control latch), thus providing controllability (another measure to represent testability). **Figure 6** shows a flip-flop circuit with a CCL structure. While the master loop is deactivated by a switch, values are written from a sense line driver. The CX-ArrayTest, which provides ATPG (automatic test pattern generation) by means of the above-mentioned controllability, also allows ATPG on asynchronous circuits.

Kawasaki Steel's KG2H and KE2H series are the first 0.8 μm ASCP products supporting the CX-ArrayTest with controllability. In addition, the Kawasaki Steel KS2H series, with its unique structure, provides the first standard cell in the world to support the CX-ArrayTest.

3.4 BIST Circuits and Boundary Scan Circuits

3.4.1 BIST circuits

In addition to the CX-ArrayTest, other means have been developed to facilitate tests. Large scale ASICs in many cases include memories such as RAMs and ROMs. Since the memories involve defect modes different from those in ordinary logic circuits, special test patterns called marching and checkers must be impressed on them at the time of shipment. For users unfamiliar with memories, it is difficult to prepare these test patterns, and even when they are prepared, they are generally very long, involving tens of kilo-words. The longer

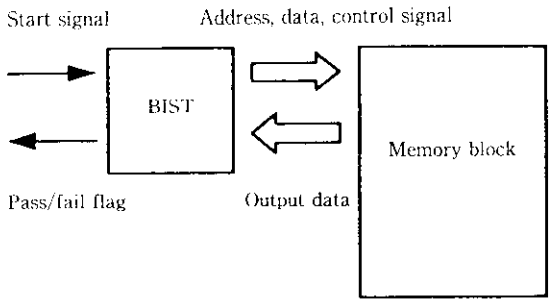

Fig. 7 Memory testing with BIST (built in self test) circuit

the test pattern, the longer an expensive ATE (automatic test equipment) will be occupied, substantially increasing test costs.

To solve these problems, a BIST (built-in self test) circuit has been developed for testing memories (**Fig. 7**). The circuit, which is provided with test pattern generation and comparison functions, can test one or more memory blocks. For the test, in addition to one exclusive test pin which is required, signal pins of ordinary circuits can be used. The BIST circuit eliminates the need for user to concern himself with memory tests. A BIST circuit is generated by a generator program to match the memory to be used by the user. Since a test pattern for the BIST circuit is also generated simultaneously, there is no need for the user to carry out to the test pattern generation for the BIST circuit.

3.4.2 Boundary scan circuits

In recent years, with the advance of narrow pitch surface packing technology, cases are increasing where conventional test methods, involving probe needle set up on a board, cannot be used. To facilitate board tests, therefore, a test method named the boundary scan method was established by JTAG, or the Joint Test Action Group (**Fig. 8**), which has been subsequently standardized as IEEE Standard 1149.1. The boundary scan method[5] is meant to test inter-LSI connections on a board and the function of an LSI itself through a test circuit prearranged inside an LSI, comprising boundary scan registers and a TAP controller.

The KG2H, KE2H, and KS2H series have scan registers uniquely structured on the chip to realize boundary scan circuits free from areal penalty and skew problems. A signal pin called TAP (test access port) which is required for a boundary scan circuit is also used as the CrossCheck CTAP (CrossCheck test access port) to minimize the penalty of an additional signal pin.

A boundary scan circuit, which is automatically software-synthesized, requires no manual design on the part of the user. Following the boundary scan register connection sequence reported at the time of automatic synthesis, users describe test patterns for board testing in BSDL (boundary scan description language) and similar languages.

3.5 Memories and Macro Functions

With 0.8 μm ASCPs, it becomes possible to integrate a number of LSIs and many MSIs on a single chip, and for large-scale ASICs such as these, it is essential to include macro functions such as memories and CPUs.

Table 3 summarizes the specifications of memories developed for the KG2H and KS2H series; all are synchronous types, designed for zero standby low power consumption. A generator program can be used to generate memories of desired sizes.

Table 4 lists features of KC80, a high speed 8 bit CPU core, developed along with the KG2H and KS2H series. The KC80, which is described in the new product column in this LSI special issue,[6] is provided with

Table 3 Specifications of memory

Product	KG2H series (gate array)		KS2H series (standard cell)	
Ttype	RAM	ROM	RAM	ROM
Control	Synchronous	Synchronous	Synchronous	Synchronous
Words	16~2 000	8~2 000	16~8 000	16~64 000
Bits	1~36	1~64	1~36	1~128
Access time[a]	10.5 ns	8.4 ns	8.5 ns	10.2 ns
Power	Zero standby	Zero standby	Zero standby	Zero standby

[a] 1 k-word × 8 b, typical condition

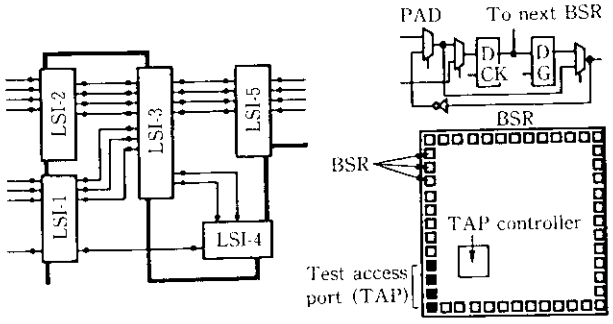

Fig. 8 IEEE 1149.1 (JTAG) boundary scan circuits

Table 4 Feature of KC80 8 bit CUP core

Items	Description
Operation voltage	2.7 V~5.5 V
Operation frequency	DC~10 MHz
Instruction fetch cycle[a]	1 cycle
External bus width	8 b
Internal bus width	16 b
Power (0.8 μm, 10 MHz)	50 mW
Instruction	Z80 compatible

[a] Typical case

object-level command compatibility with Zilog's Z80, a standard 8 bit product. However, the KC80 is tremendously improved in the view of the data throughput and the power consumption, therefore it provides ideal architecture for such applications as portable apparatus.

3.6 Low Thermal Resistance Packages

Mere reduction of power consumption of core cells to about 50% (those of 1.0 μm cells) is insufficient to fully utilize the merits offered by the high density, up to 2.4 times, of 0.8 μm ASCP products. Considering that operating frequency is becoming higher each year, measures for the package in which the chip is scaled become necessary. Accordingly a low thermal resistance plastic package with a heat spreader was developed, using a lead frame made of copper instead of conventional 42% Ni alloy. **Figure 9** graphically represents the relation between the thermal resistance of a low thermal resistance package and air velocity, showing that the low thermal resistance package has lower thermal resistance than the ceramic one.[7] While these packages are slightly more expensive than conventional plastic equivalents, they are much cheaper than ceramic ones, and further cost reduction is expected with future volume production.

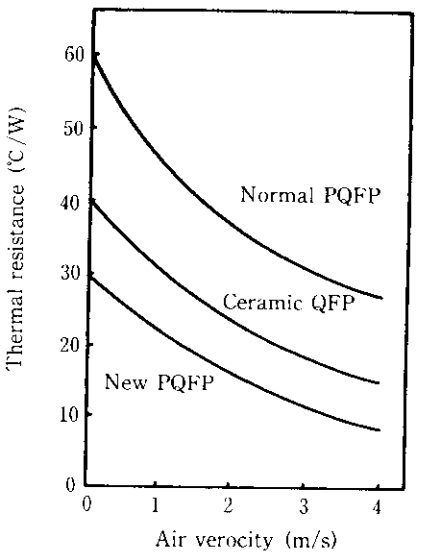

Fig. 9 Thermal resistance characteristics of packages

4 Application Examples

4.1 Image Processor

An image processor chip has been developed which processes a 5 × 5 pixel window by means of the KG2H series. **Figure 10** shows the image processor, consisting of a 14.5 k bit SRAM and 12 k gate random circuit, and its block diagram. The power consumption is about 300 mW, representing a reduction of approximately 60% from that of the 1.0-μm series. **Figure 11** shows the relation between the number of test patterns which are generated by the CX-ArrayTest and fault coverage, representing a comparison between conventional manual test pattern generation and fault simulation. The CX-ArrayTest easily provides substantially higher fault coverage, 95% or higher at 5 k words.

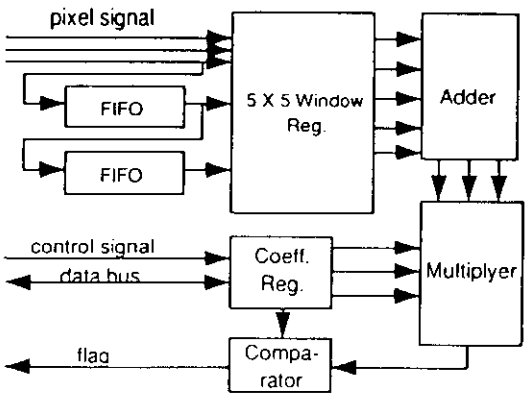

Fig. 10 Block diagram of image processor

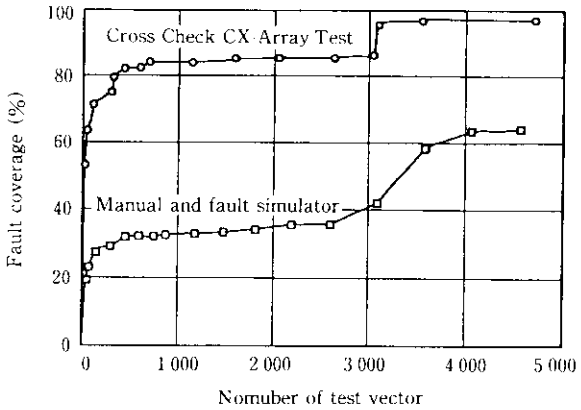

Fig. 11 Comaprison of fault coverage between CX-ArrayTest and normal method

4.2 Multi-processor

Using the KG2H series, a multi-processor (**Photo 1**) consisting of seven KC80s has also been developed. **Figure 12** shows the block diagram. The multi-processor, which includes two 64 k bit SRAM blocks, is structured so that the master processor controls six slave processors. High density core cells capable of structuring memories efficiently have made possible a gate array with a large scale system including about a million transistors.

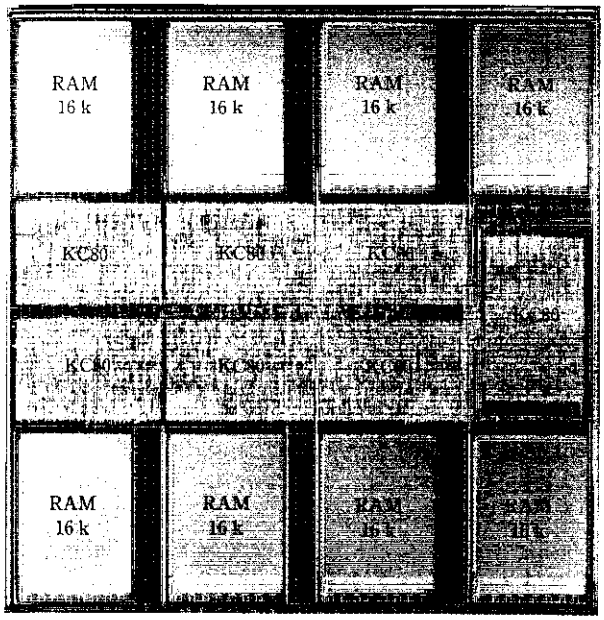

Photo 1 Multi processor chip

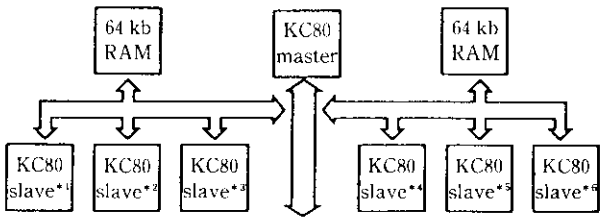

Fig. 12 Multi processor system

5 Conclusions

(1) 0.8 μm ASCP products have been developed, which are designed to solve the problems of increased power consumption and testing difficulties encountered in structuring large scale LSIs.
(2) Macro functions such as memories and CPU cores have been developed as well to provide the functions necessary to structure large scale systems.
(3) Chips such as image processors and multi-processors have been designed and their efficiency verified.

In addition to the next generation 0.5 μm ASCP products now being developed, it is our intention to continue introducing unique products accurately reflecting the needs of users.

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