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# Overview of ASIC Technology and Business

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The recent advancement of information processing technology has been achieved by the use of the ever increasing capabilities of ICs. Different application technologies, e.g., consumer electronics, computers and telecommunications are merging to form an entire new world of information technology that is recognized as accelerating a change of social structure. This special issue on LSIs reviews Kawasaki Steel Corporation's technology and business structure in the field of ASICs (application specific integrated circuits) that support the advancement of electronic equipment through higher functions and increased density.



The body can be viewed from the next page.

# Overview of ASIC Technology and Business*

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## 1 Introduction

In the past 20 years, the information processing capacity of communication and computers has increased by more than a million times. Thanks to this improvement, electronic digital information, once restricted to numerals and characters, has extended into the areas of pictures and voice as well, and consolidation of high speed information networks will enable free exchange of information including moving pictures beyond the boundaries of time and distance (**Fig. 1**). It is considered that such progress in information processing technology is revolutionizing not only the industrial structure but also the foundation of society.[1]

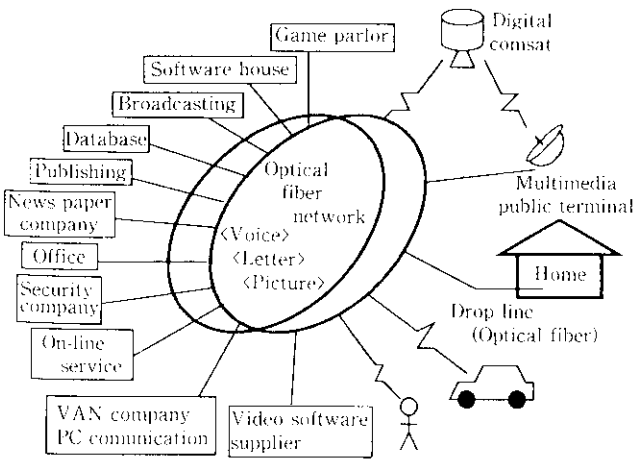


Fig. 1 High speed network

Information processing technology is bases on the advance of IC (integrated circuit) technology and software technology. The performance of the MOS transistors that comprise an IC is improved with decreased transistor geometry, which is the target of manufacturing process development, and also contributes to improved cost performance of ICs. In turn, improved cost performance of ICs through advanced manufacturing technology and expanded demand through the development of new areas of applications, working as two inseparable factors, have supported the rapid growth of the electronic industry.

In the history of the electronics industry, memories and processors have been the driving force for IC technology. At the same time, an increasing need for ICs designed for specific applications, and for ASICs (application specific integrated circuits) in particular, has accelerated ASIC technology. While IC memory is regarded as a technology driver for the manufacturing process and device structures, ASIC technology has a wider technology base, including manufacturing, logic design, architecture design, and system design. The LSI business of Kawasaki Steel focuses on CMOS-ASICs. Therefore, technology and the business of CMOS-ASICs will be reviewed in this paper.

## 2 ASIC Market Trend

### 2.1 Types of ASICs

**Figure 2** shows the broad classification of LSI products. ASIC is a general term for ASSPs (application

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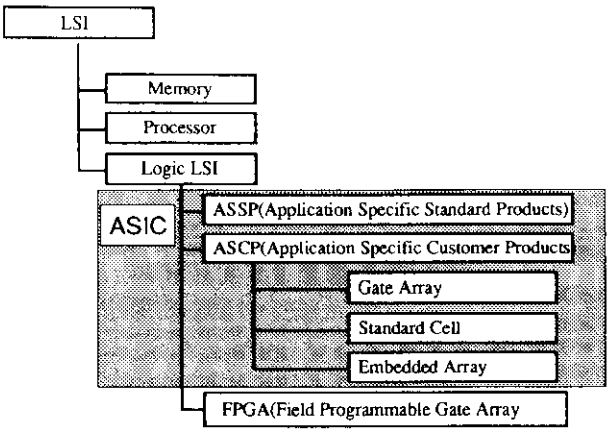


Fig. 2 Different types of ASICs

specific standard products) and ASCPs (application specific customer products). FPGAs (field programmable gate arrays) and PLDs (programmable logic devices), which allow user programming, are not included.

In the case of ASSPs, manufacturers determine the LSI specifications. Not only do they design and manufacture LSIs, but they also determine how LSIs are applied in users' equipment systems. The manufacturers provide information, technical documents, demonstration boards, and evaluation software which users require in designing their equipment. ASSPs are sometimes supplied together with firmware that is also built into users' systems.

In the case of ASCPs, users specify LSI applications, determine their specifications and, in many cases, make logic designs as well. Design of ASCPs is performed using CAD systems supplied by ASIC manufacturers. Depending on their intended application, users choose either gate arrays, standard cells, or embedded arrays, of which the differences are described below.

(1) Gate Array
This is a metal-programmable type of IC. Transistors regularly arranged on a base array are connected with metal layers to provide a logic function. Since the circuit can be modified easily by simply changing the metal placement, this method contributes to shorter development time.

(2) Standard Cell
A macro cell is designed on arbitrarily laid out transistors. While densities 30–40% higher than those of gate arrays can be realized, circuit modification involves changes in transistor layout, hence a full process must be run to obtain sample ICs. This will result in higher costs and require more time than in the case of gate arrays.

(3) Embedded Array
Portions that require no modifications are designed in the form of a standard cell and embedded in the base array of a gate array. Densities higher than those of gate arrays can be realized, and circuit modification is facilitated.

It is an important function of ASCP manufacturers to work out a system that can provide the LSIs required by users with the minimum turnaround time. Such systems include design system (CAD and library) as well as a manufacturing process which ensures delivery of qualified products in a short period of time.

There exists a vertical relationship in which ASCP manufacturers provide ASSP manufacturers with the LSI designing environment necessary for ASSPs. Recently, however, advances in ASCP design technology have prompted a move among ASSP manufacturers to have their own ASCP design environments. ASCP manufacturers, in the meantime, have begun to meet increasingly sophisticated needs for ASIC design through the automatic generation of general purpose circuits such as memories and data paths, and strengthened support for system design, including the provision of CPU cores (**Fig. 3**).

### 2.2 Requirements of ASIC Market

ASICs are developed as a part of equipment develop-

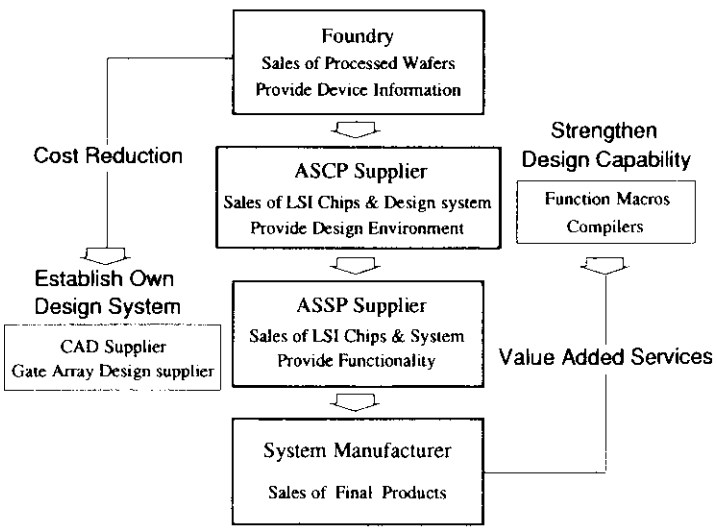


Fig. 3 Players in ASIC businesses and trend in customer-supplier relationship

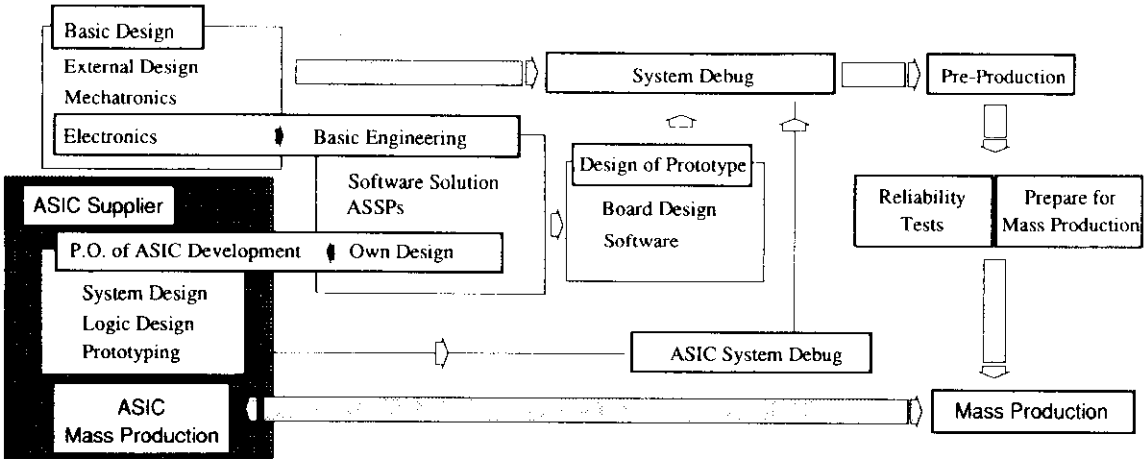


Fig. 4 ASIC business as a part of electronic equipment business

ment (**Fig. 4**). In an increasingly competitive market, equipment manufacturers must continue to develop products superior to those of their competitors in an ever shorter turnaround time. It is incumbent upon ASIC manufacturers to constantly provide the optimum solution to this problem.

The electronics industry, as it enters the 21st century, is expected to make rapid progress toward:

(1) Consolidation and development of communication networks
(2) Increased miniaturization of equipment
(3) Integration of different information (multimedia)

ASICs are expected to meet these different needs by providing new signal processing functions and on chip integration of multiple functions. **Figure 5** shows the gate counts by function of LSIs for portable wireless multimedia terminals expected to be commercialized by around 2000. Further development in ASIC technology, both in manufacturing and designing, is desired so that highly integrated LSIs, on which multiple functions are integrated, can be designed quickly and produced at competitive prices.

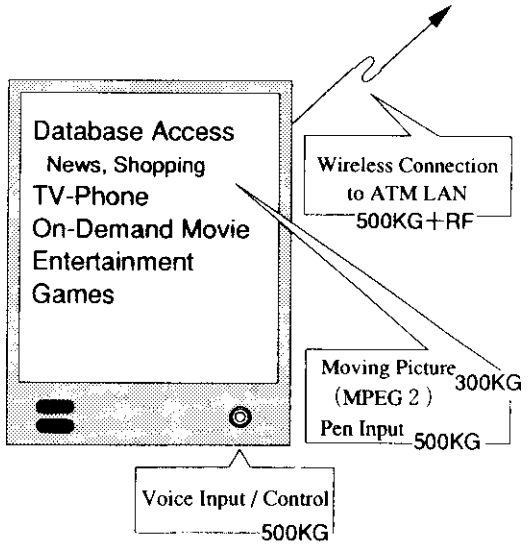


Fig. 5 Portable wireless multimedia terminal and gate count estimate to perform independent functionality

## 3 Perspectives on ASIC Technology

As described above, market requirements are tending toward shorter turnaround time for development, miniaturization of equipment, and cost reduction. ASIC technology has been developed as a means to realize these requirements.

With particular emphasis on these three points, perspectives on ASIC technology will be described in the following.

### 3.1 Shorter Development Turnaround Time

To reduce development time, ASIC manufacturers offer two solutions: extension of an ASSP into subsystems, and provision of technology to shorten the ASCP development time.

Examples of ASSPs extended into subsystems include modems, graphic accelerators, and voice response wireless ATM interface, as shown in Fig. 5. Using this kind of subsystem ASSP can minimize the risk associated with system development.

Shorter ASCP development time calls for both hardware and software approaches. As the scale of ASCPs is expanded and more sophisticated systems are integrated, LSI system verification will take up an increasing portion of the overall development time.

Among the different types of ASCPs, gate arrays are particularly suitable to shorten a development cycle involving trial manufacturing, system verification, and circuit modification. High density gate array technology is a hardware solution to overcome low available gate count, which is a weakness of traditional gate arrays as compared with other ASICs.

Functions that cannot be provided by gate arrays are

served by embedded arrays. By fixing memory and analog sections, of which the specifications can be determined with relative ease as early as the stage of system design, and designing a logic circuit with gate arrays, requirements for more sophisticated functions and shorter development time can be satisfied.

Software to shorten the development time can be summarized into the provision of properly verified functional macros and the CAD technology to realize them. The basis of the CAD technology to design LSIs has almost been perfected. Since it is necessary to continue improving the CAD technology to accommodate LSIs with larger scales and circuits with higher speeds, further development of advanced logic synthesis,[2] simulators, faster automatic placement and routing,[3] and technology to facilitate test is expected.

The core of the future CAD technology may shift to a new type of CAD that allows system verification[4] as well as LSI design verification in an integrated design environment. Technology to verify systems without using test-produced LSIs is an important means to reduce the development time of final products.

### 3.2 Miniaturization of Equipment (System-On-Silicon Technology)

**Figure 6** shows how the ASCP technology has typically evolved. Increased available gate count through the development of processes, and advanced design and CAD technologies have promoted the integration of subsystems.

To realize multi-functional information terminals as described above, it is necessary to integrate many processing functions on a single LSI. To make this type of LSI, which is called a system-on-silicon, parts on a board, or individual LSIs must be integrated on a silicon substrate. In addition to a design environment

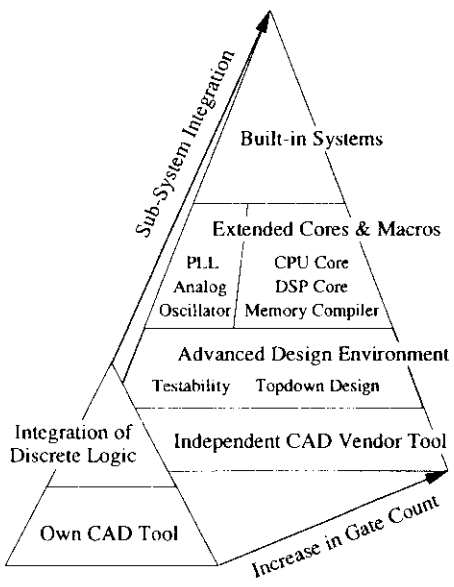


Fig. 6 Progress in ASCP technology

Table 1 Examples of general purpose function cell for the system on silicon

| | |
|---|---|
| Proccesor | CPU core<br>Digital signal processor<br>Peripheral |
| Memory | RAM/ROM<br>Non-volitle memory |
| Functional macro | Adder/Subtracter<br>Multiplier/Divider<br>Digital filter<br>DCT engine |
| Clock generater | Crystal OSC<br>Phase locked loop |
| Interface | Bus driver<br>ADC/DAC |

including the above system verification, standard parts are made available in the form of macro cells (**Table 1**).

### 3.3 Cost Reduction (Process and Device Technology)

The process generation of DRAMs changes every three years. In the past three generations (nine years), the bit count of single DRAMs has increased by 64 times, while the area increase has remained at about 3.5 times. The density improvement is at about 2.5 times per generation[5]. Per bit DRAM prices have continued to drop by about 26% per year[6] with the increased density realized by generation changes working as a motive force for the simultaneous improvement of performance and cost.

The same improvement in cost performance is attainable in ASICs with finer process generation rules. It is a function of ASIC manufacturers to provide LSIs having good cost performance and advanced information processing capacity. **Figure 7**, a Dataquest report, shows the design start windows of CMOS gate arrays in different process generations, along with total available gates.

The ASIC manufacturing process is different from that of memories in that the ASIC manufacturing process:

(1) Requires multi-layer metals, in addition to processes particular to memories,
(2) Can accommodate irregular transistor and metal placement.

Compared with memories, ASICs involve irregular placement of metals between transistors, and longer metal length per transistor. Accordingly, the density of ASICs (shown in the number of transistors per unit area or gate counts) depends on the number of metal lines per unit area. The number of metal lines per unit area can be increased either by reducing the metal pitch or by increasing the number of metal layers.

A process generation is normally represented by the

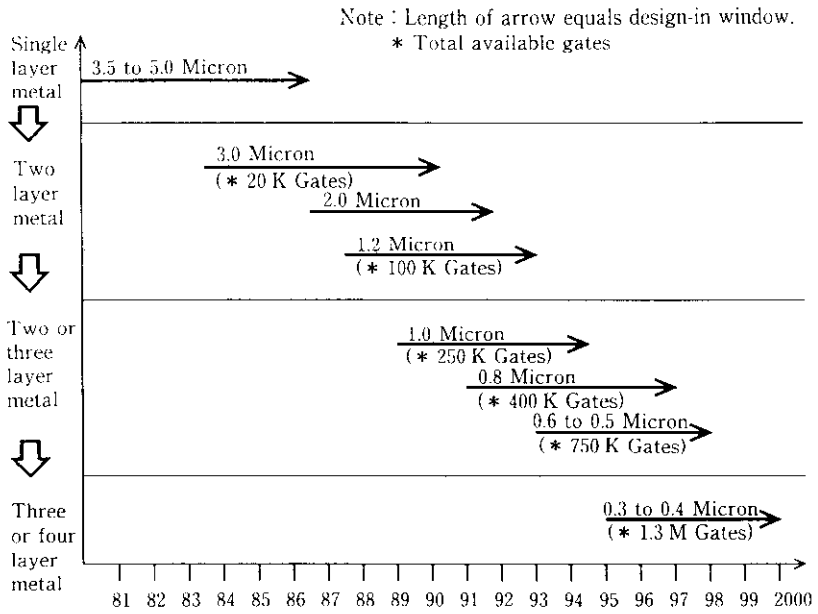


Fig. 7 CMOS gate array start technology road map (Source: Dataquest, December 1992)

minimum processable dimension. The basic performance of CMOS transistors depends on the gate length, which is ordinarily equal to the minimum processable dimension. It is therefore customary to use the gate length to represent a process generation. Because the minimum dimensions of other parts of CMOS transistors, even of the same generation, differ according to process design, they must be optimized to match intended ASICs. For cost reduction, a process is advantageous that can reduce the number of metal layers and increase the metal line density.

## 4 Development of Kawasaki Steel's ASIC Business

Our LSI business has been focused on ASICs. It is our prime objective to serve our customers in this fast growing sector of the electronics industry and to participate in a part of the development of advanced equipment. As described in this special issue on LSIs, the products we have been developing are now ready to serve the specific requirements of variety of customers.

It is important to provide a design environment suitable for developing large scale subsystems to meet the future needs of the ASIC market. On the basis of this perception, our LSI business is geared to meet customers' need by providing large scale ASICs at competitive prices.

The distinctive points of our LSI business can be summarized as follows:

(1) High density gate arrays to meet the requirements of advanced applications on the basis of our original processes and architecture optimized for ASICs
(2) ASICs with designed-in test facility circuits developed by CrossCheck Technology Inc.
(3) Top-down design environment, including advanced CAD systems through cooperation with Cadence Corporation
(4) 8 bit CPU core and peripherals which operate in a fully static mode and are designed for easy use in ASIC design
(5) A series of ASSPs which are specific to communication and imaging applications, but can also be used as ASCP cores

## 5 Conclusions

LSIs are aptly considered the fundamental element of industry, and in fact form the basis of every industry today. The foregoing has reviewed the market and technology with respect to ASICs, a type of LSIs on which this company places particular emphasis.

This special issue on LSIs suggests, Kawasaki Steel Corp. will proceed with its new LSI business. We trust that it will also be taken as expressing our will to contribute to the growth of the LSI industry.

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